Use of ALD and selective isotropic etch / ALE in the manufacturing of advanced logic and memory devices

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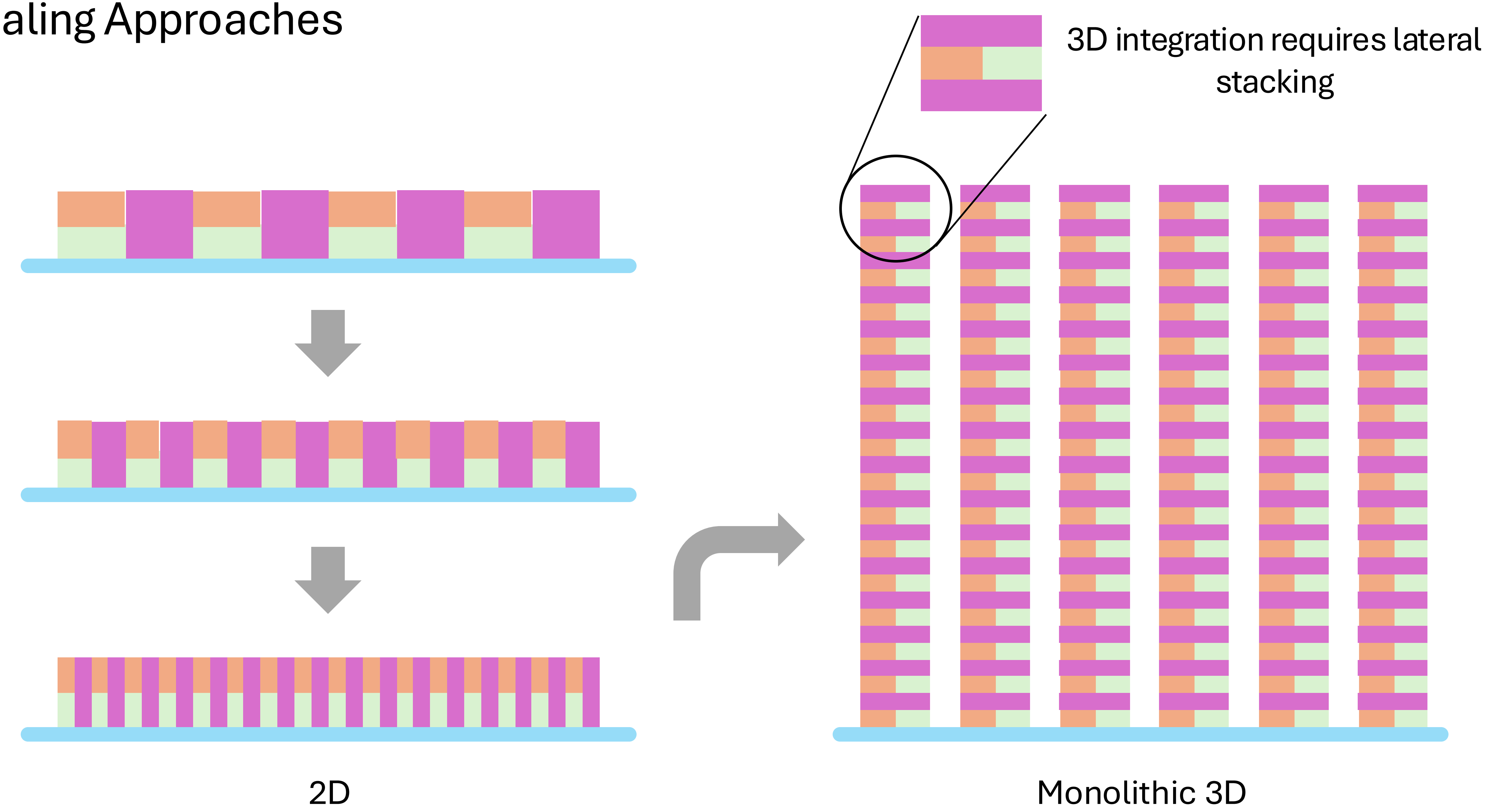
Outline

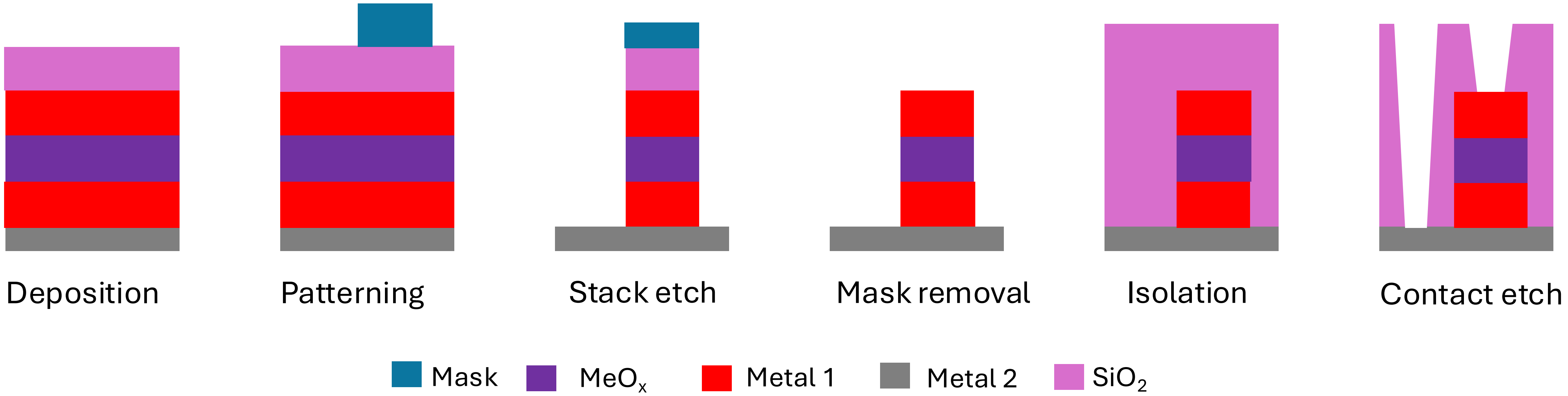
- Introduction
- Patterning with Atomic Scale Fidelity: Use of ALD and ALE
- Deposition and etch technologies
- Formation of High Aspect Ratio Scaffolds: HAR Dielectric Cryo Etch
- Lateral Stacking: ALD and selective isotropic etch / ALE
- Application examples

Scaling Approaches



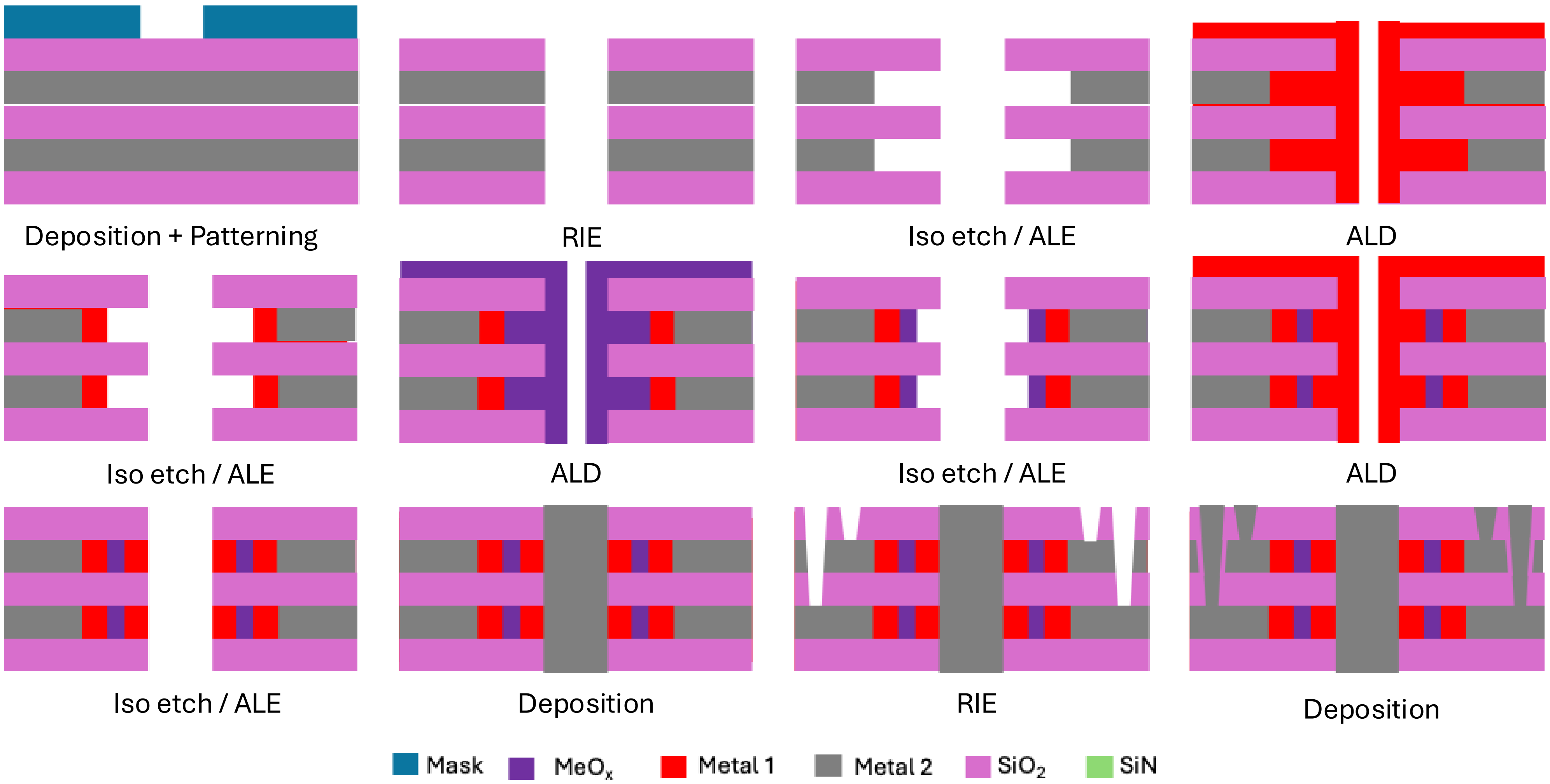
Conventional 2D Integration

Example of ReRAM memory cell with two electrodes and metal oxide memory layer



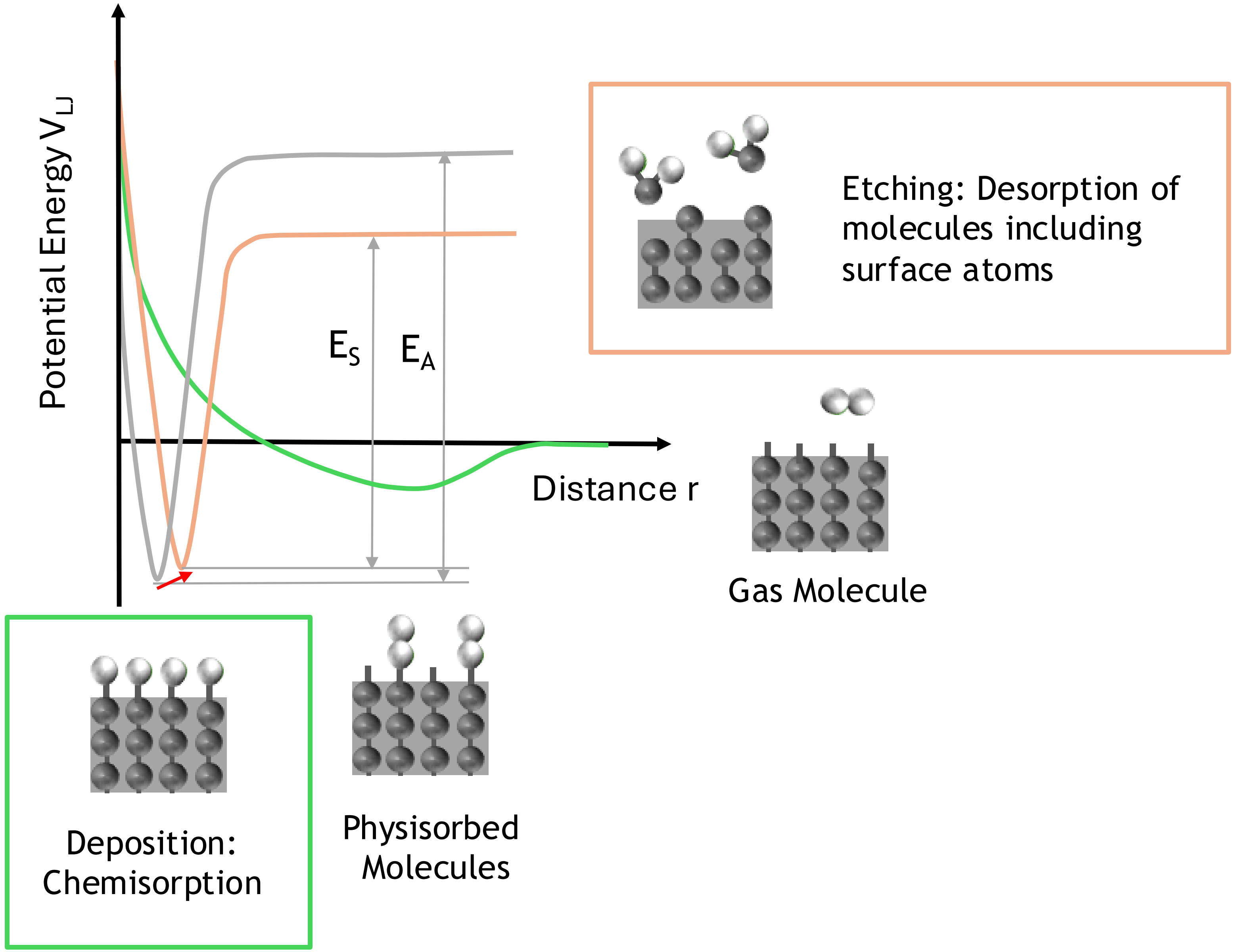
2D integration requires top-down vertical etch and deposition.

Conventional 2D Integration

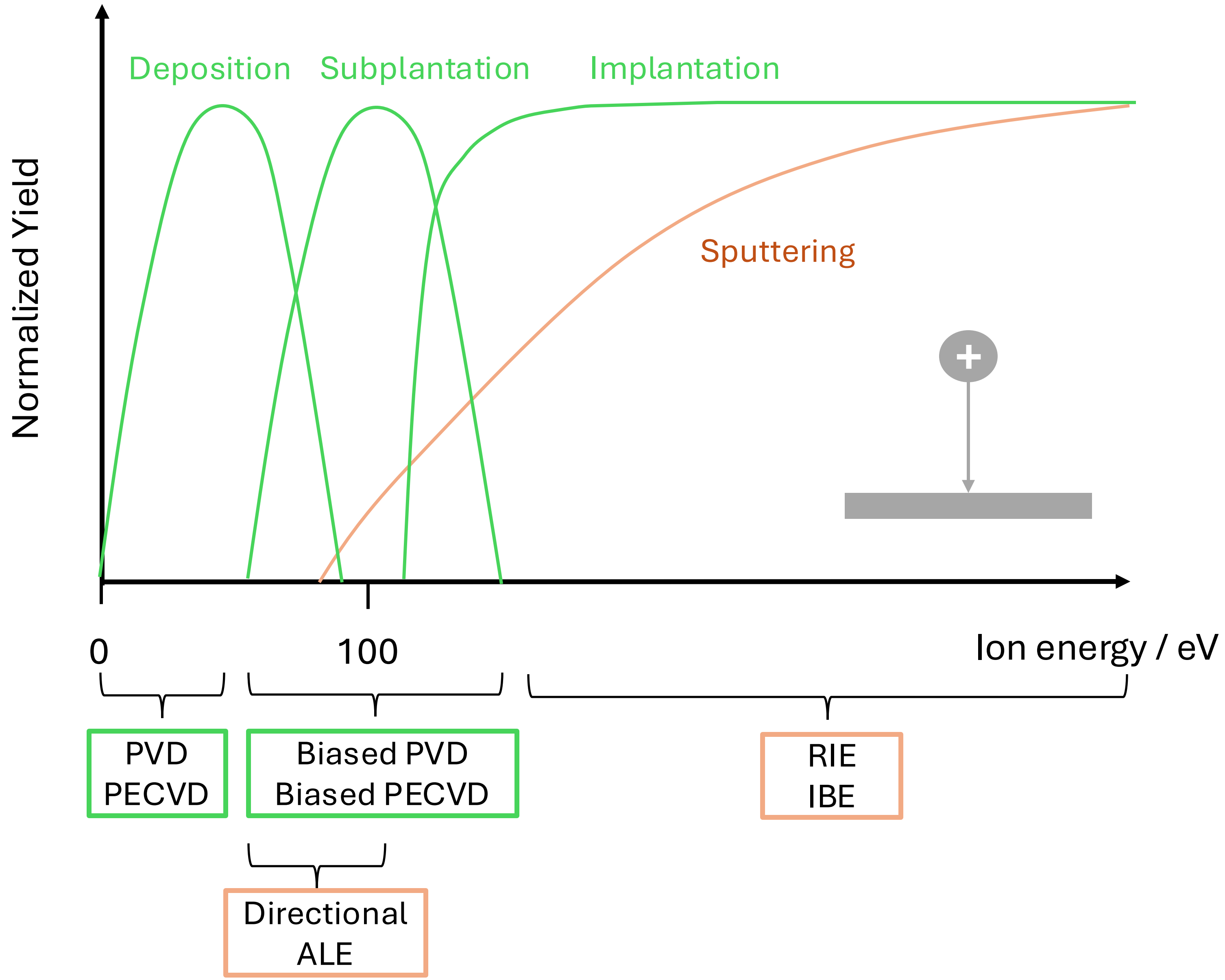


3D integration requires vertical and lateral etch and deposition.

Deposition and Etching: Chemistry Aspects



Deposition and Etching: Physics Aspects



Deposition:
Energies of several eV to overcome activation barrier

Subplantation:
Penetration in the top layers of a growing film with the goal to change structure and increase film density. Widely used in carbon deposition.

Implantation:
Deep penetration accompanied by sputtering. Can be used to modify the composition of a deposited film.

Sputtering:
Ejection of surface atoms at the end of a collision cascade. Onset of sputtering at the sputtering threshold (several 10 eV).
Sputtering yield increases with the square root of the ion energy.
Direction ALE used difference in threshold for modified and original material.

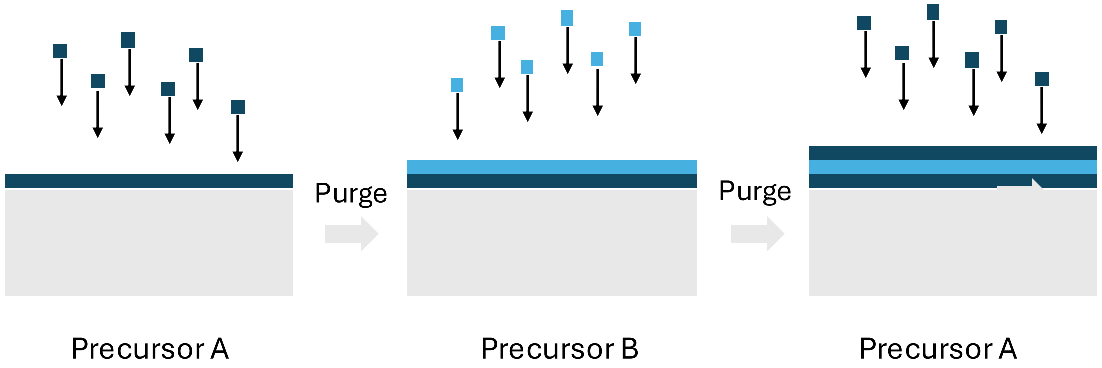
Vacuum Deposition and Etch Technologies

Deposition	Continuous	Physical Vapor Deposition (PVD)	Plasma Enhanced Chemical Vapor Deposition (PECVD)		Low Pressure Chemical Vapor Deposition (LP CVD)
	Cyclic Self-limited		Plasma Enhanced Atomic Layer Deposition (PE ALD)		Thermal ALD; Epitaxy
Etch	Continuous	Ion Beam Etching (IBE)	Reactive Ion Etch (RIE)	Radical Etching	Thermal Etching
	Cyclic Self-limited		Directional Atomic Layer Etch	Plasma Enhanced Isotropic ALE	Thermal Atomic Layer Etching (Thermal ALE)

Physics ⟷ Chemistry

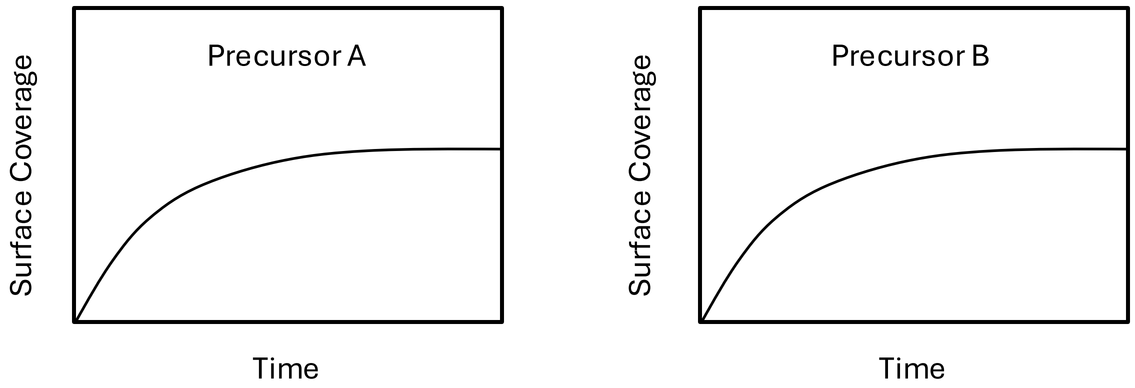
Atomic Layer Deposition

Temporal and special separation of two half-reactions:

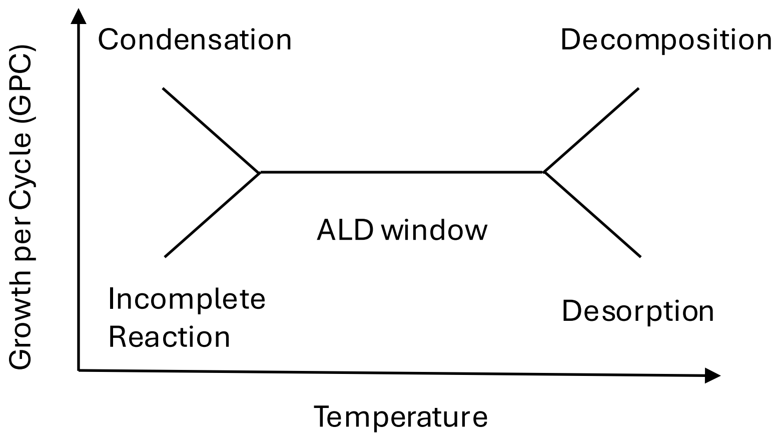


Example Al_2O_3 ALD:
Precursor A: $Al(CH_3)_3$
Precursor B: H_2O

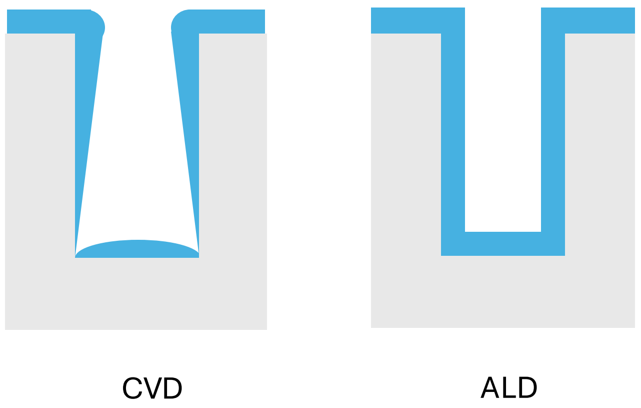
Self-limited or saturated half-reactions:



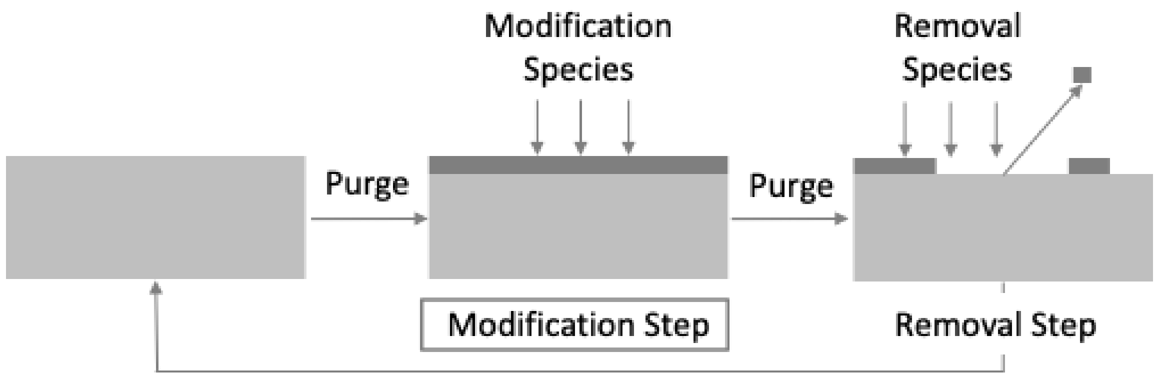
Ideal ALD window:

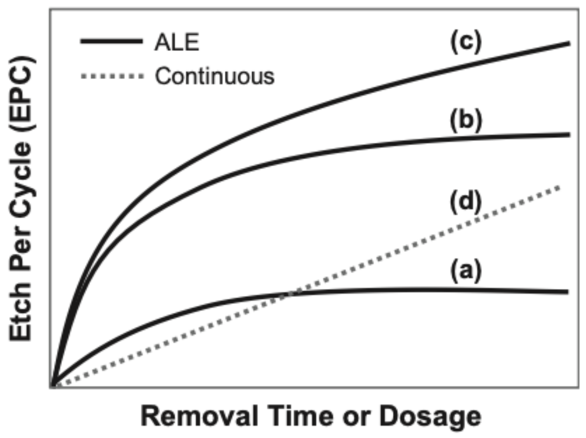


ALD Benefit: Conformality

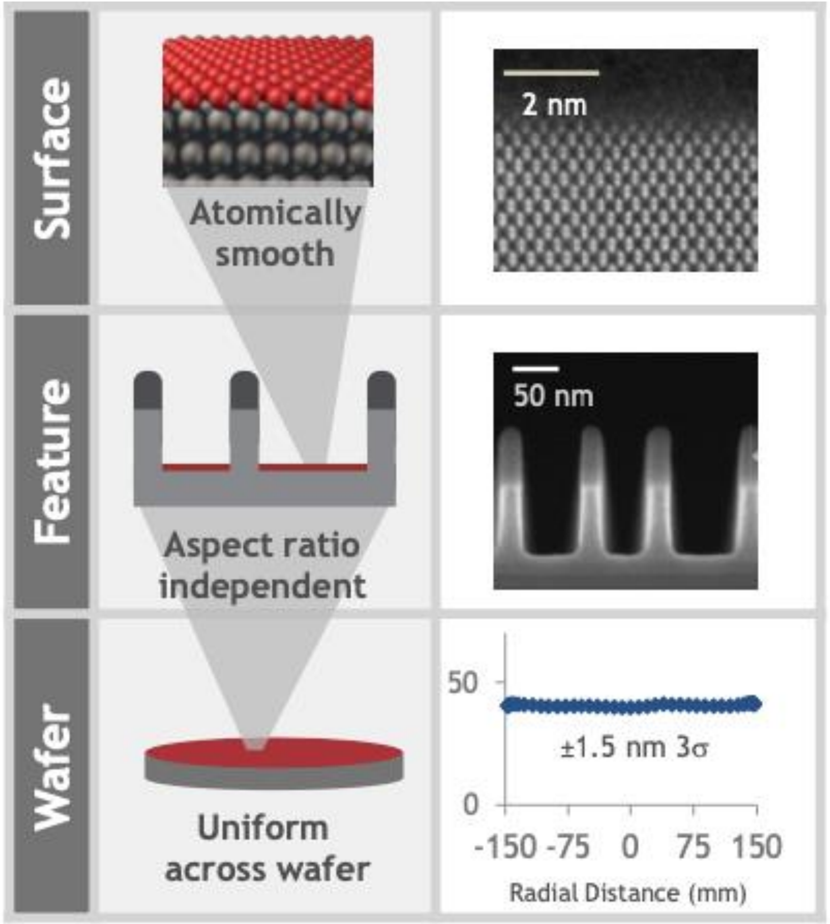


Directional Atomic Layer Etch



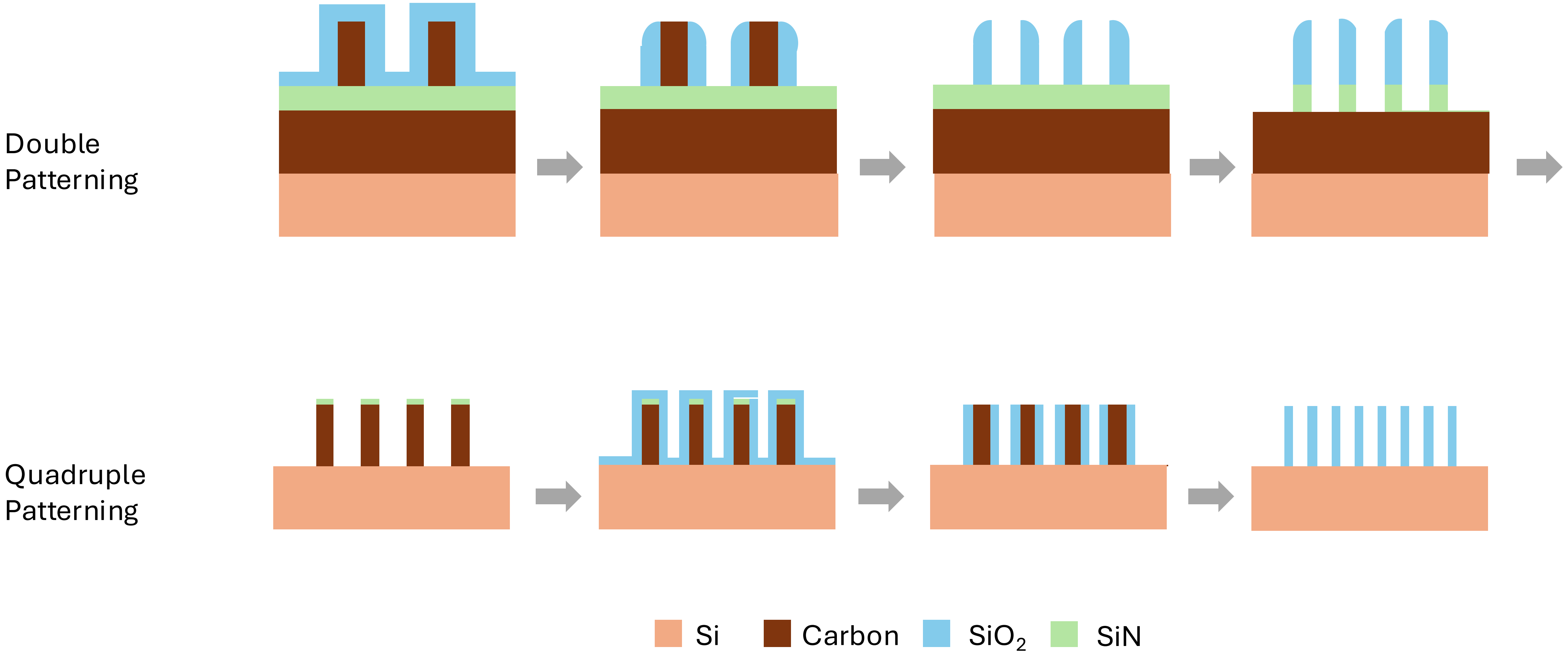


K. Kanarik et al., *J. Vac. Sci. Technol. A* 33, 020802 (2015).

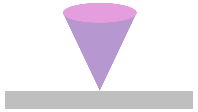
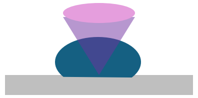
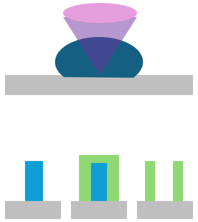
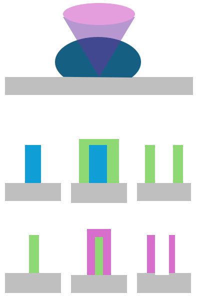
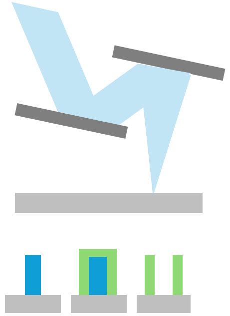


ALE addresses RIE challenges by separating modification and removal into self-limited steps.

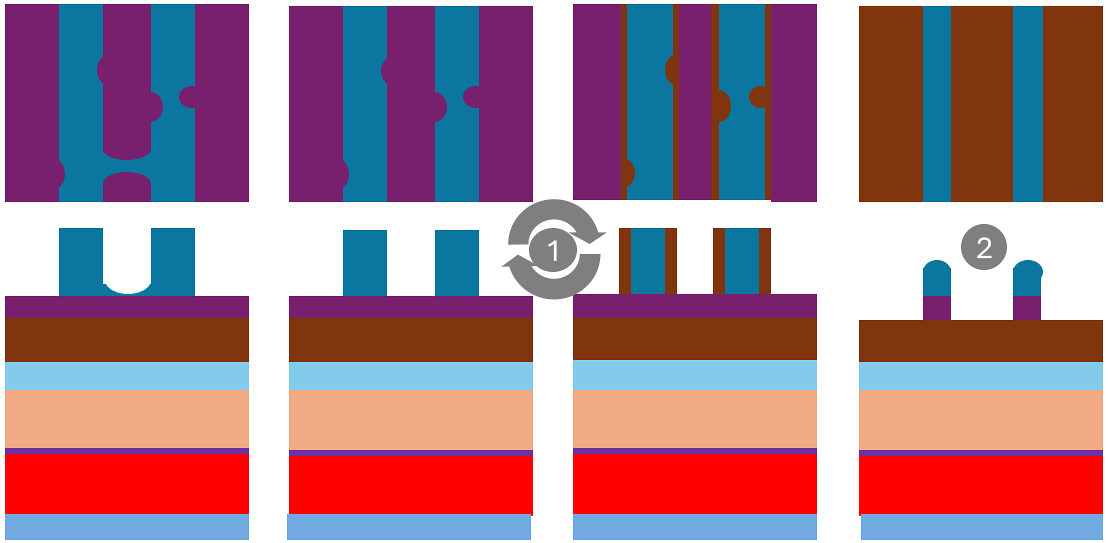
Self-aligned Multiple Patterning



Patterning Evolution (Logic Devices)

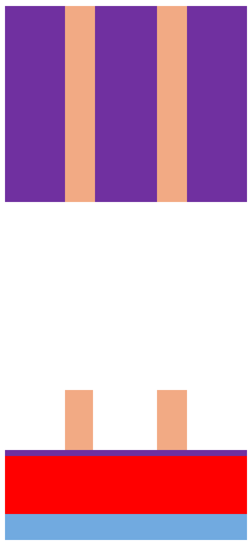
First year HVM	2000	2010	2012	2014	2018	2020	2025
Node	130 nm	32 nm	14 nm	10 nm	7 nm	5 nm	2 nm
Patterning Technology	DUV SP 	Immersion DUV SP 	Immersion DUV DP 	DUV QP 	0.33 NA EUV SP 	EUV DP 	0.55 NA EUV SP 
ALD application			• SiO_2 spacer dep	• Enhanced spacers (new materials, grated composition)		• Enhanced spacers (new materials, grated composition)	• Vapor phase infiltration
Potential ALE application				• Spacer etch	• EUV resist treatment • Underlayer open • Mask open	• EUV resist treatment • Underlayer open • Mandrel open • Spacer etch	• EUV resist treatment • Underlayer open • Mask open

ALD and ALE Applications in EUV Double Patterning (BEOL TiO_2 hardmask)



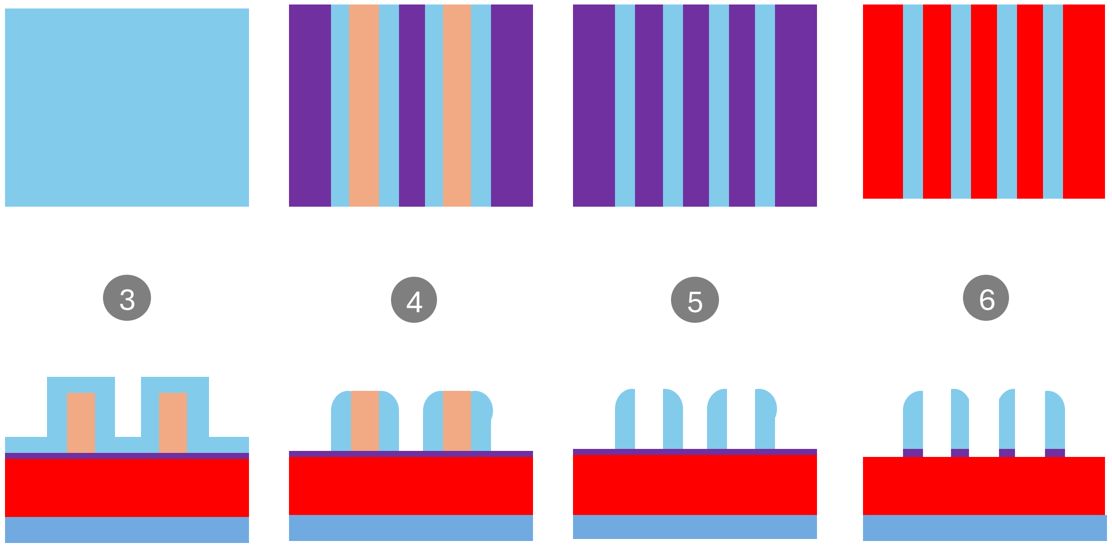
Underlayer open

1. Line edge smoothening with ALE type carbon deposition / removal cycles
2. Directional ALE for dielectric underlayer opening selective to EUV resist



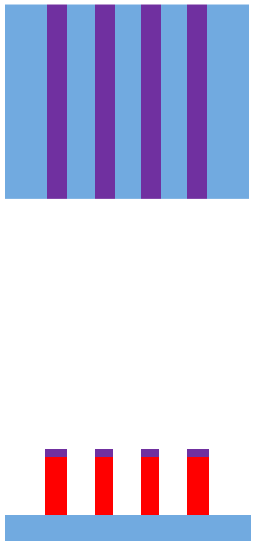
Mandrel etch

RIE is sufficient. Cryo etch has been demonstrated to have superior line bending performance.



Double Patterning

3. ALD SiO_2, SiN or Metal oxide ALD
4. Directional ALE for spacer opening selective to etch stop.
5. Thermal ALE for mandrel pull
6. Directional or thermal ALE for etch stop open

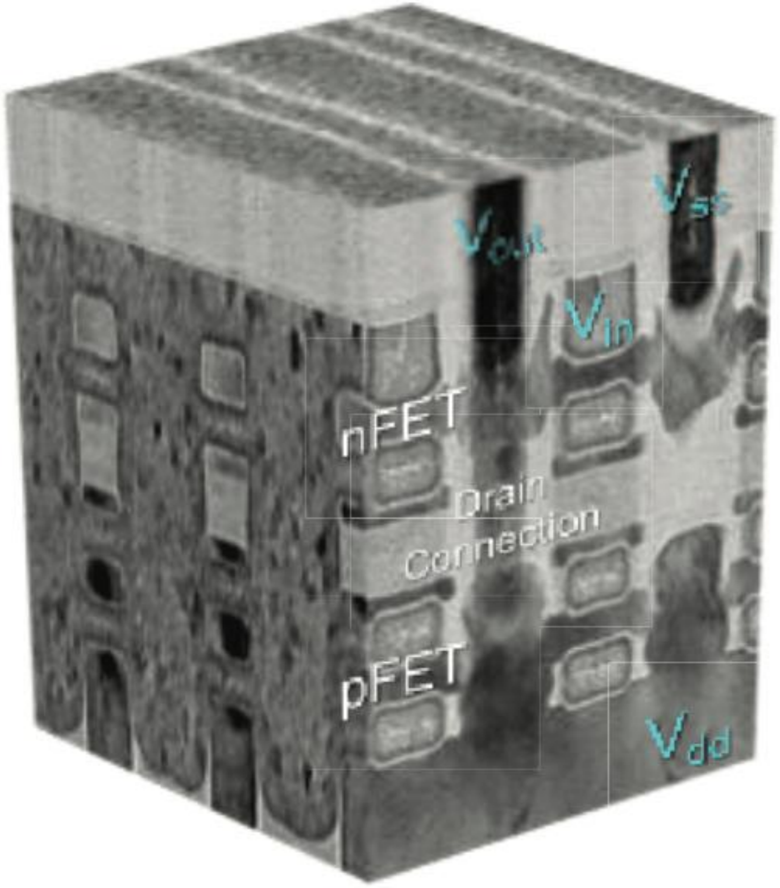


Mask etch

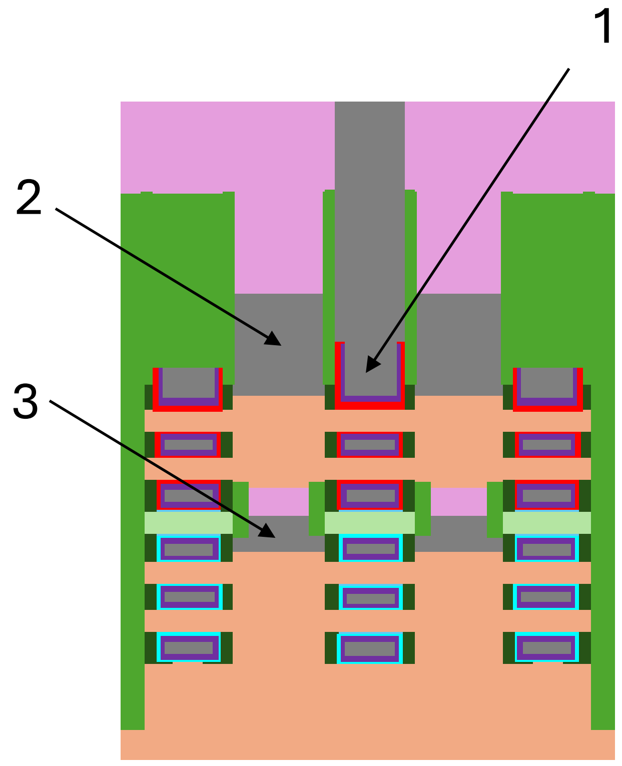
RIE is sufficient. Line is proportional to ion energy. Directional ALE could be option. ALD deposition of the mask can reduce internal stress and reduce line bending.

Si | TiO_2 | DUV PR | Carbon | EUV underlayer | SiO_2 | Non-volatile etch stop | Low k dielectric

How to utilize deposition and etch technologies to realize complex 3D devices?



Mii (tsmc), IEDM 2024



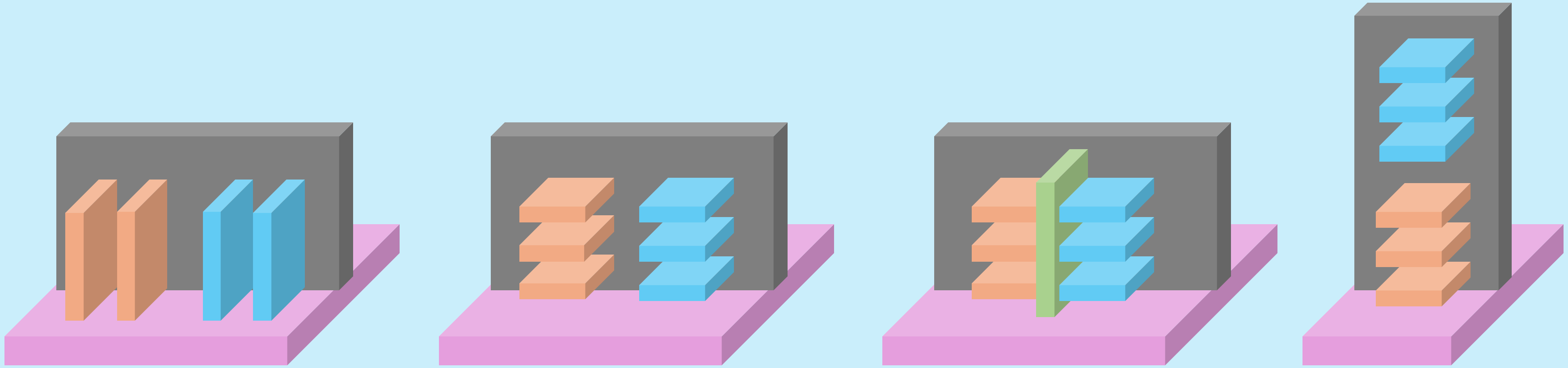
1 – gate
2 – top contact
3 – bottom contact

Si   SiGe SiO_2 SiN   SiCO(N)   other SiN material)

WF Metal 1   WF Metal 2   High k   W

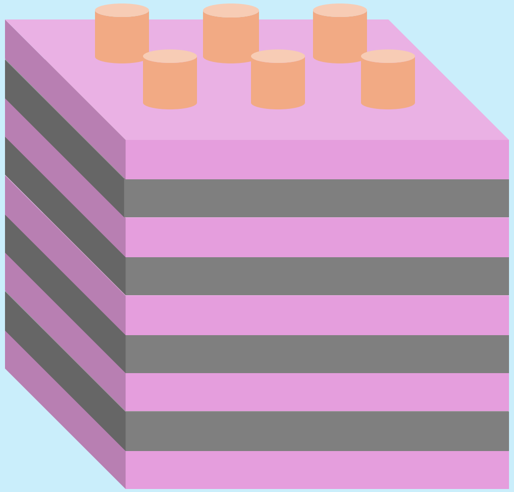
3D Devices: The era of ALD and isotropic selective etching / ALE

Logic

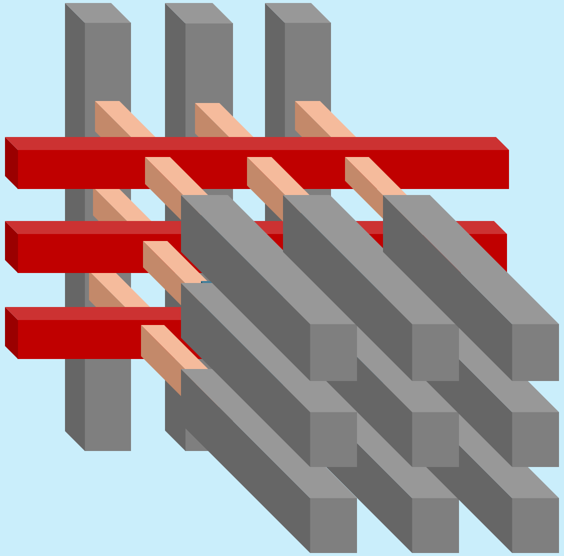


Flash

ReRAM
PCRAM
FERAM

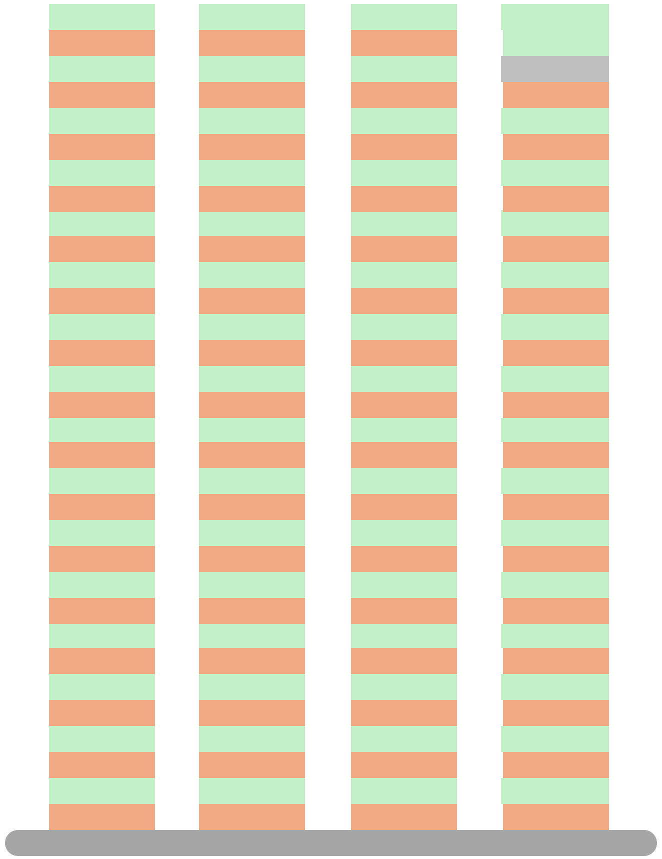


DRAM



The need for lateral processing drives demand for ALD and isotropic selective etch.

Scaffold Materials

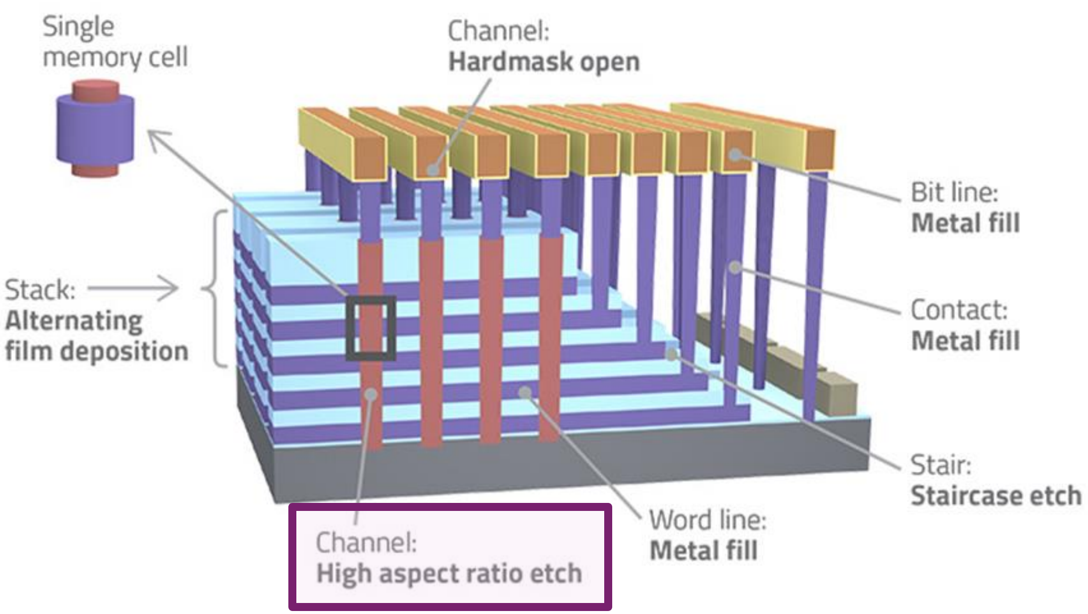


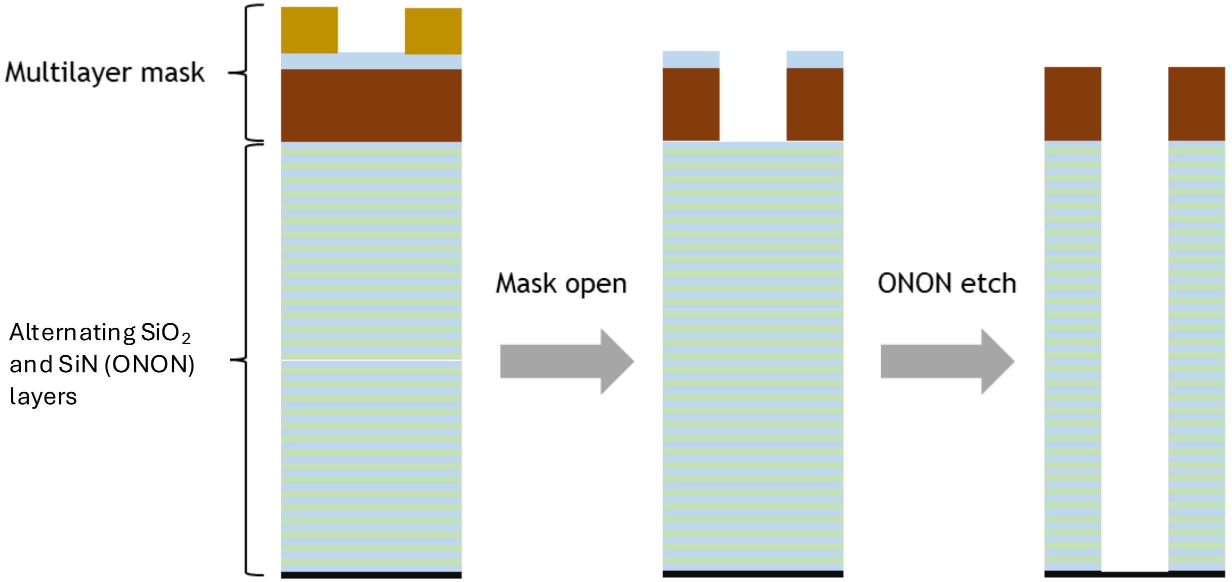
Key building block for 3D devices is a structure which houses transistor and/or memory devices

- *Comprised of at least two materials*
- *One material is dielectric. Another material can be conductor or sacrificial material*
- *Etching properties drive the use of silicon-based materials*
- *Etching of tall SiO_2 / metal stacks are very hard to etch with high etch rate*
- *Typical stacks and deposition methods:*

Stack	3D Device	Layer Replacement	Stack Deposition method
SiO_2 / SiN (ONON)	RG NAND	SiN → W, Mo	PE CVD
SiO_2 / poly-Si (OPOP)	GF NAND	n/a	PE CVD
Si / SiGe	3D DRAM	SiGe → SiO2, SiN, metals	Epitaxy
Si / SiGe	GAA FET, CFET	SiGe → metals, SiN	Epitaxy

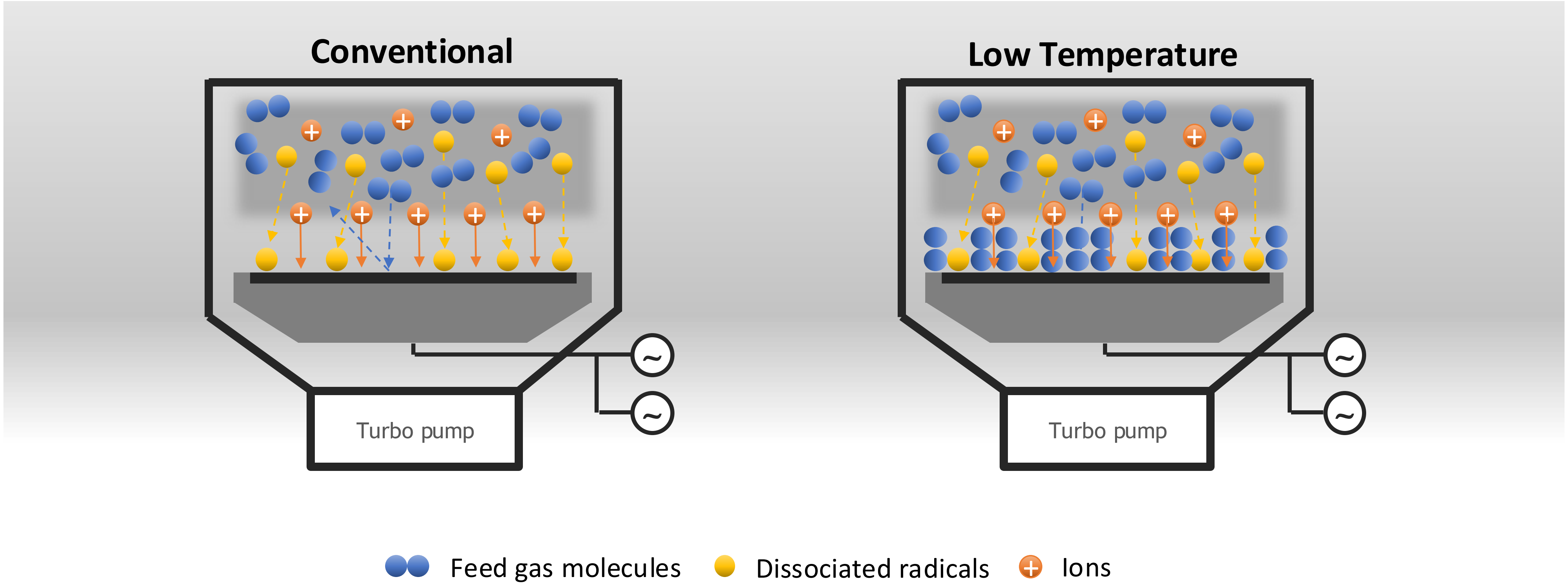
High Aspect Ratio Etching of SiO_2/SiN for 3D NAND Memories





- *Industry is ramping 2xx layers and roadmaps to 5xx SiO_2/SiN layers have been announced.*
- *Aspect ratios are approaching 100.*
- *The path to 1000 layers will be etched (https://newsroom.lamresearch.com/1000-layers-NAND-etch).*
- *Novel etch solutions are needed.*

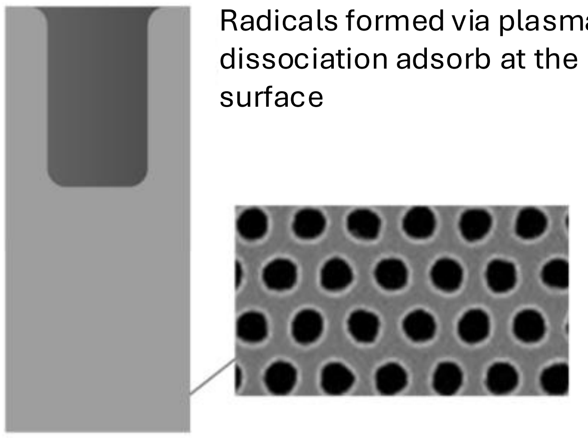
High ONON Dielectric Etching Rate at Lower Temperature



Surface coverage can be increased at low temperatures when non-dissociated species can physisorb.

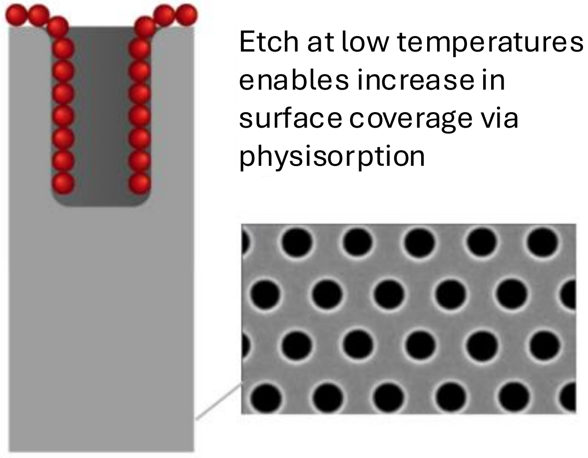
Cryo^{TM} Etch Benefits for High Aspect Ratio SiO_2/SiN Etching

Cryo^{TM} 1.0



Radicals formed via plasma dissociation adsorb at the surface

Polymerizing chemistry causes irregular mask and hole shapes



Etch at low temperatures enables increase in surface coverage via physisorption

"Lean" chemistry results in regular mask and hole shapes

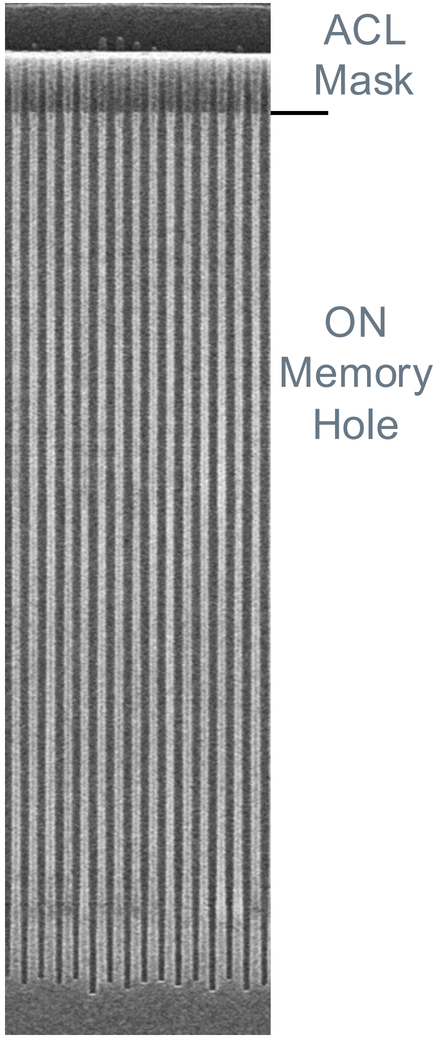
Cryo^{TM} 1.0:

- Higher etch rate
- Better mask morphology

"Scaling to 1,000-Layer 3D NAND in the AI Era", Counterpoint Research and Lam Research White Paper July 2024

Cryo^{TM} 2.0 | Cryo^{TM} 3.0

Profile Deviation (max-min/depth)	0.2%
Depth	>8 µm



Cryo^{TM} 2.0:

- Further increased etch rate

Cryo^{TM} 3.0:

- Uniform hole diameter top to bottom

H.Singh, Semicon West, July 2024

Active Materials: Logic, DRAM, NAND, Power and Optical Devices

Material Class	Material	ALD	Dir. ALE	Iso ALE
Silicon compounds	Si			
	SiGe			
	SiO_2			
	SiN			
	SiC			
	SiCO			
	SNC			
III-V semiconductors	GaAs			
	GaN			
	GaNAl			
2D materials	WS_2			
	WSe_2			
	MoS_2			
	$MoSe_2$			
	Graphene			
Carbon and carbon polymers	amorphous carbon			
	carbon based polymers			

Material Class	Material	ALD	Dir. ALE	Iso ALE
Metals and metal alloys	W			
	Mo			
	Ru			
	TiAl			
	GeSbTe			
	OTS (GeAsTe, GeSe, GeTe)			
Metal oxides	HfO_x			
	Al doped HfOx			
	ZrO_x			
	$HfZrO_x$			
	La doped $HfZrO_x$			
	LaO_x			
	Y_2O_3 incl. Eu, Er doping			
	TiO_x			
	TaO_x			
	AlO_x, AlO_xN_x			
	NbO			
	SnO			
	InGaZnO, InO_x			
Metal nitrides	TiN			
	TaN			
	WNxCy			

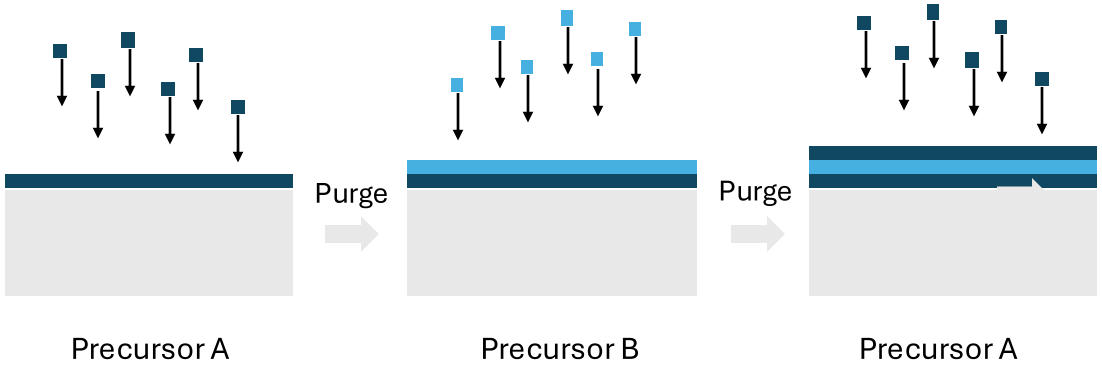
Source:
ALD: 2020 – 2024 IEDM, VLSI and SPIE Advanced Lithography Symposia
ALE: 2020 – 2024 IEDM, VLSI and SPIE Advanced Lithography Symposia and predictions by author

Active Materials by Memory Type

		Flash	3D DRAM	RRAM (CB, Ox)	FeFET memory	PCRAM
Transistor	Channel	Poly-Si	Single cryst. Si	Poly-Si	Poly-Si, IGZO	Single cryst. Si
	Gate oxide	SiO_2, HfO_x	SiO_2, HfO_x	SiO_2	$HfZrO_x$	SiO_2, HfO_x
	Gate	W, Mo	W, Mo	Poly-Si	W	Poly-Si
	Charge trap	SiN, HfO_x				
Resistor	Electrode	n/a	n/a	W, TiN, Zr, Ti	n/a	W
	Variable resistor			HfO_x, TiO_2, Ta_2O_5		GST: GeSbTe OTS: GeAsTe, GeSe, GeTe
Capacitor	Electrodes		W	n/a		n/a
	Dielectric		High k dielectric			

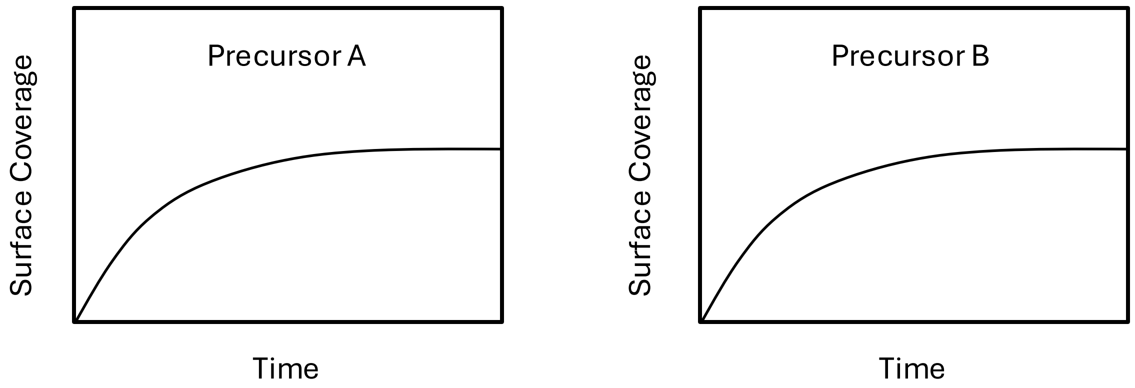
Atomic Layer Deposition

Temporal and special separation of two half-reactions:

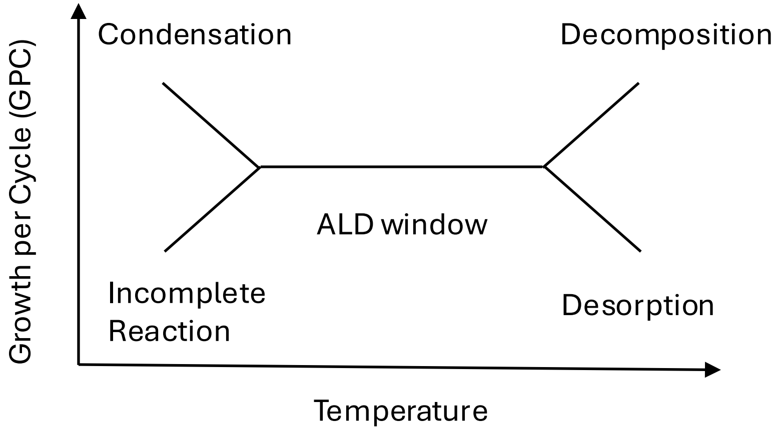


Example Al_2O_3 ALD:
Precursor A: $Al(CH_3)_3$
Precursor B: H_2O

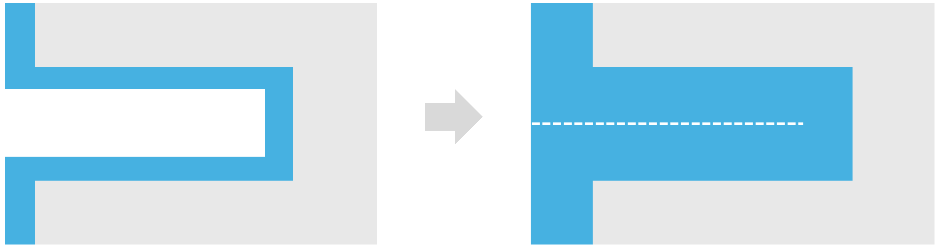
Self-limited or saturated half-reactions:



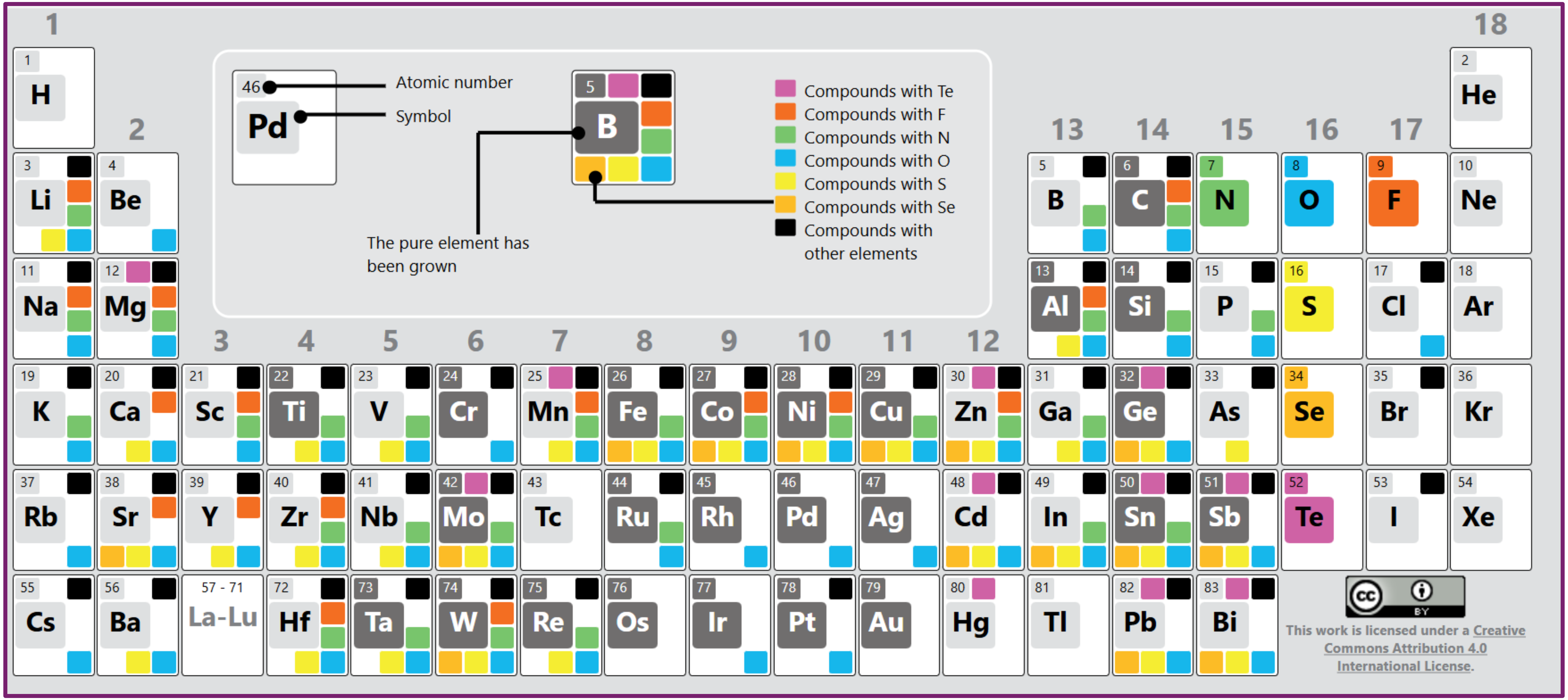
Ideal ALD window:



ALD Benefit: Lateral Gapfill



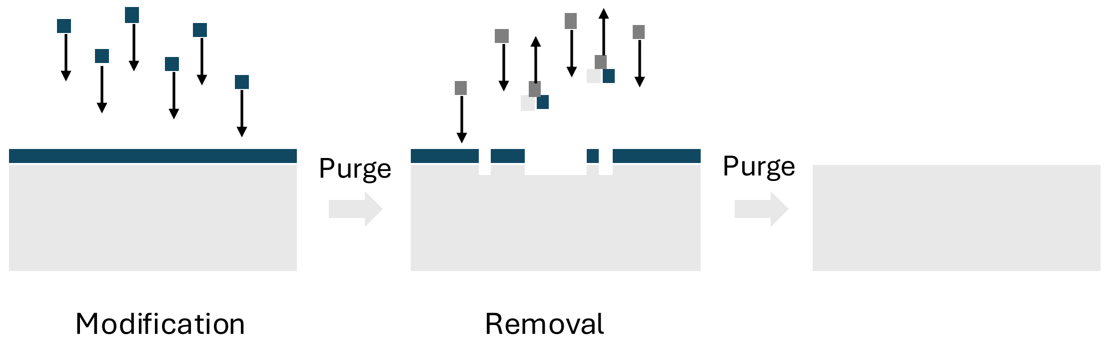
ALD Database



"Atomic Limits" database is regularly updated at www.AtomicLimits.com.

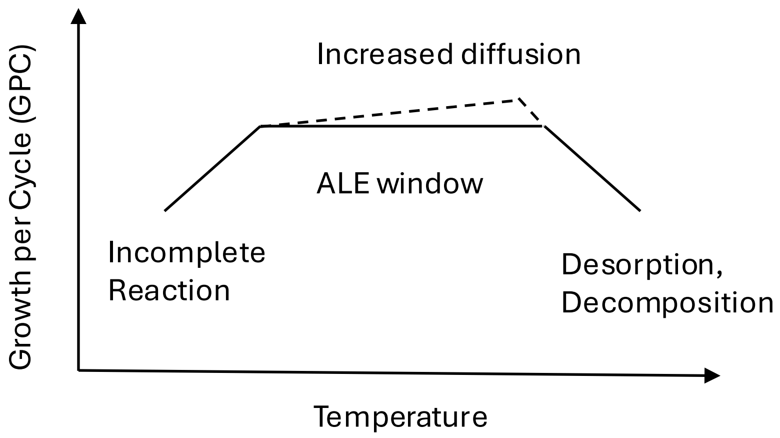
Selective Isotropic Etch: Thermal Atomic Layer Etch

Temporal and special separation of two half-reactions:

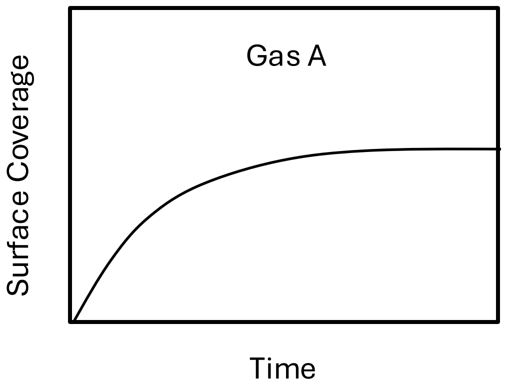


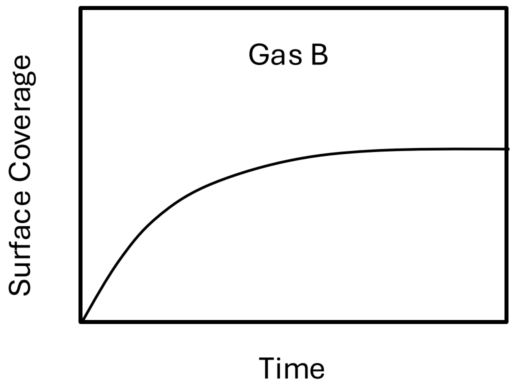
Example Al_2O_3 ALE:
Precursor A: HF
Precursor B: $Al(CH_3)_3$

Ideal ALE window:

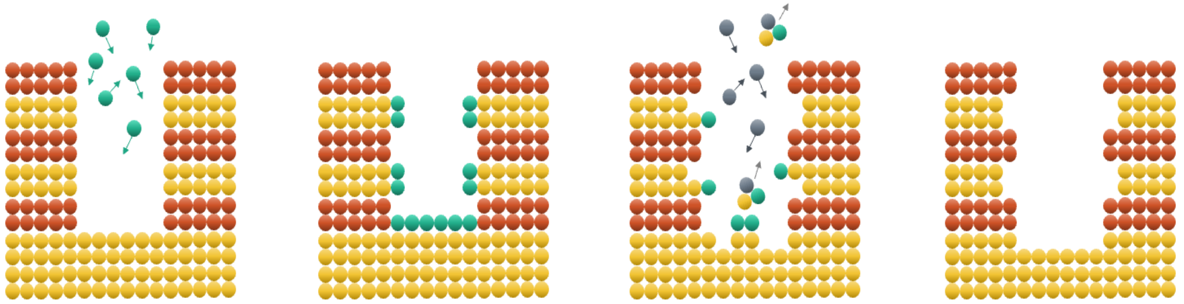


Self-limited or saturated half-reactions:

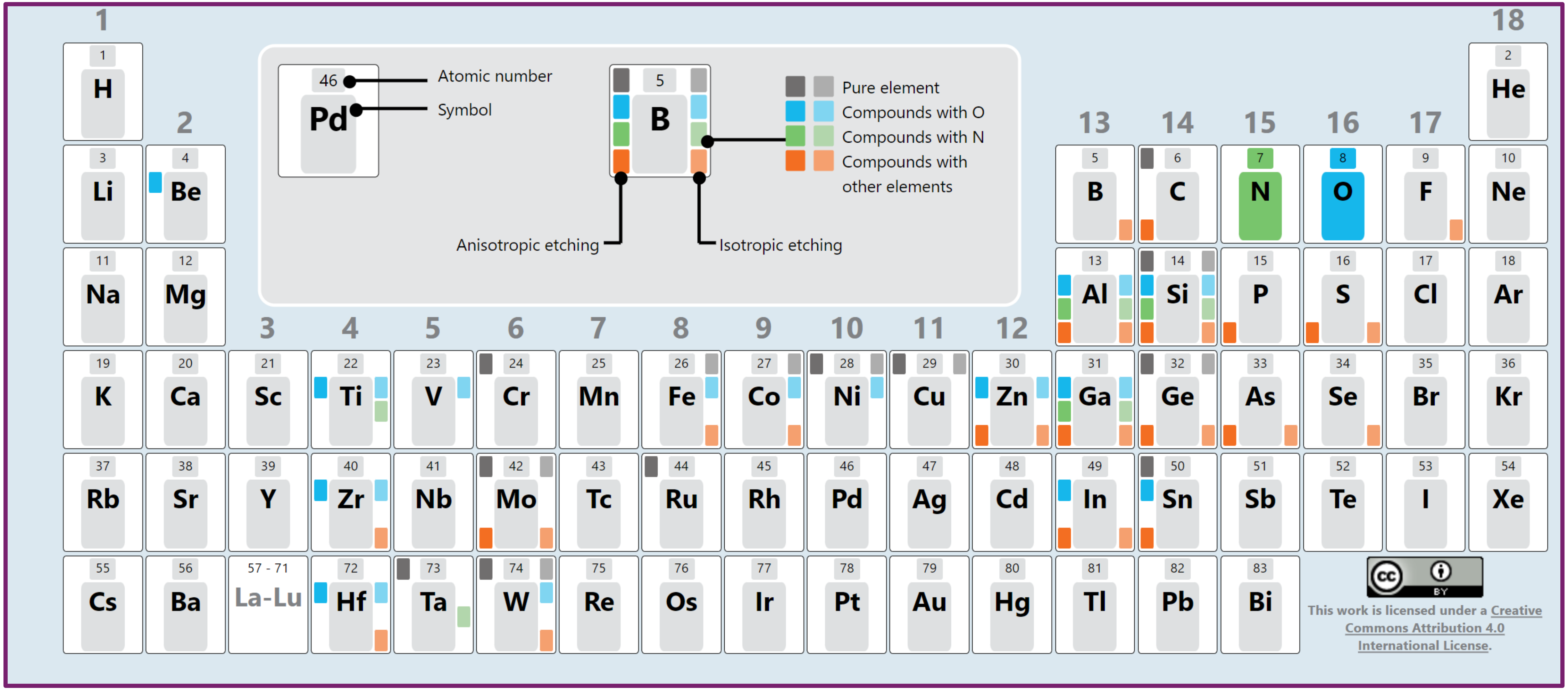




ALE Benefit: Isotropy, Top – Bottom Uniformity

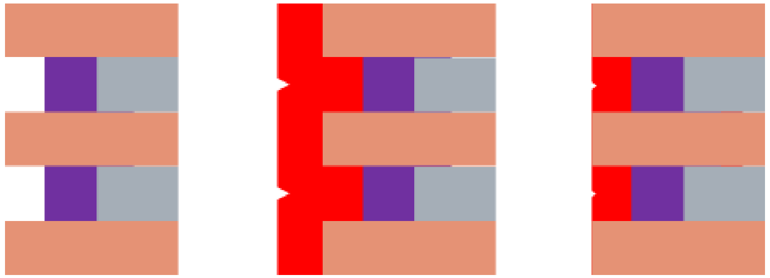


ALE Database

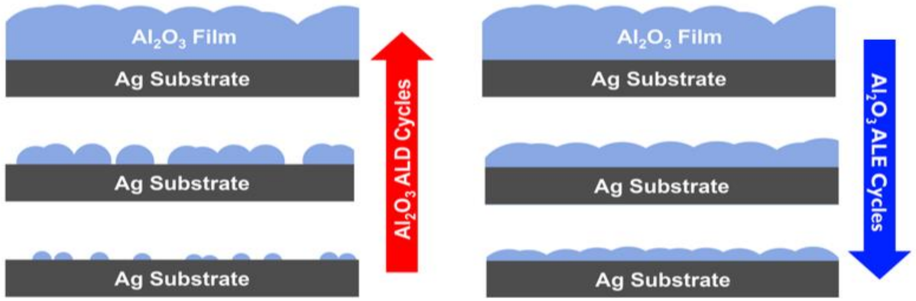


"Atomic Limits" database is regularly updated at www.AtomicLimits.com.

Novel capabilities combining ALD and Selective Etch / ALE

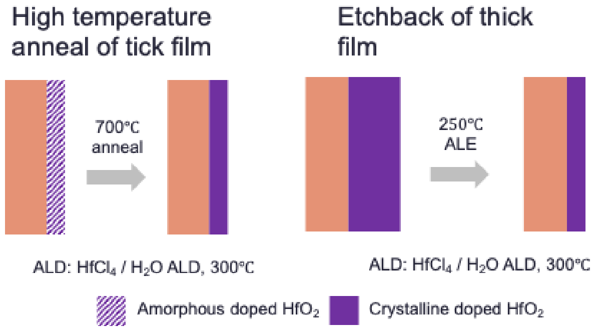


Lateral integration



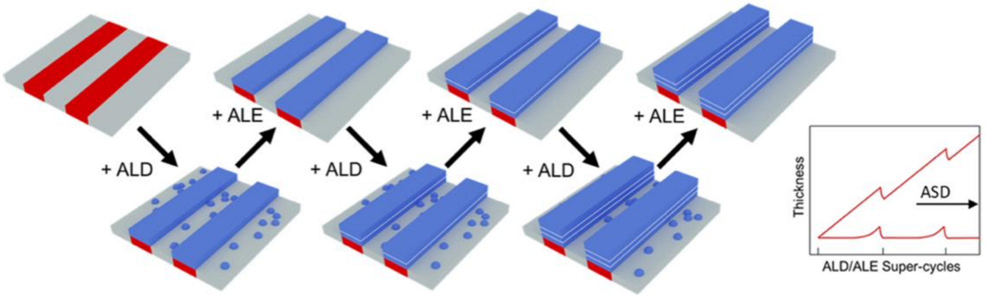
Smooth thin films

Gertsch et al.; J. Vac. Sci. Technol. A **39** (2021) 062602



Crystalline thin films

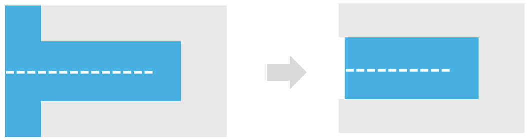
Yurchuk et al., Thin Solid Films **533**, 88 (2013)



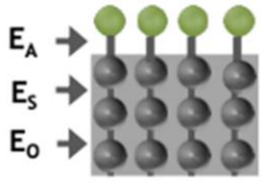
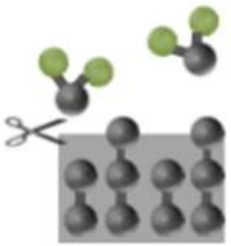
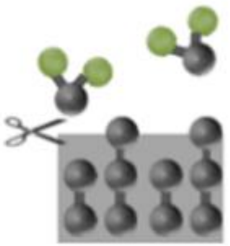
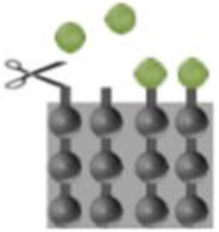
Area selective deposition

Song et al.; Chem. Mater. **31**, 4793 (2019)

Selective Isotropic Etch: Thermal Etch

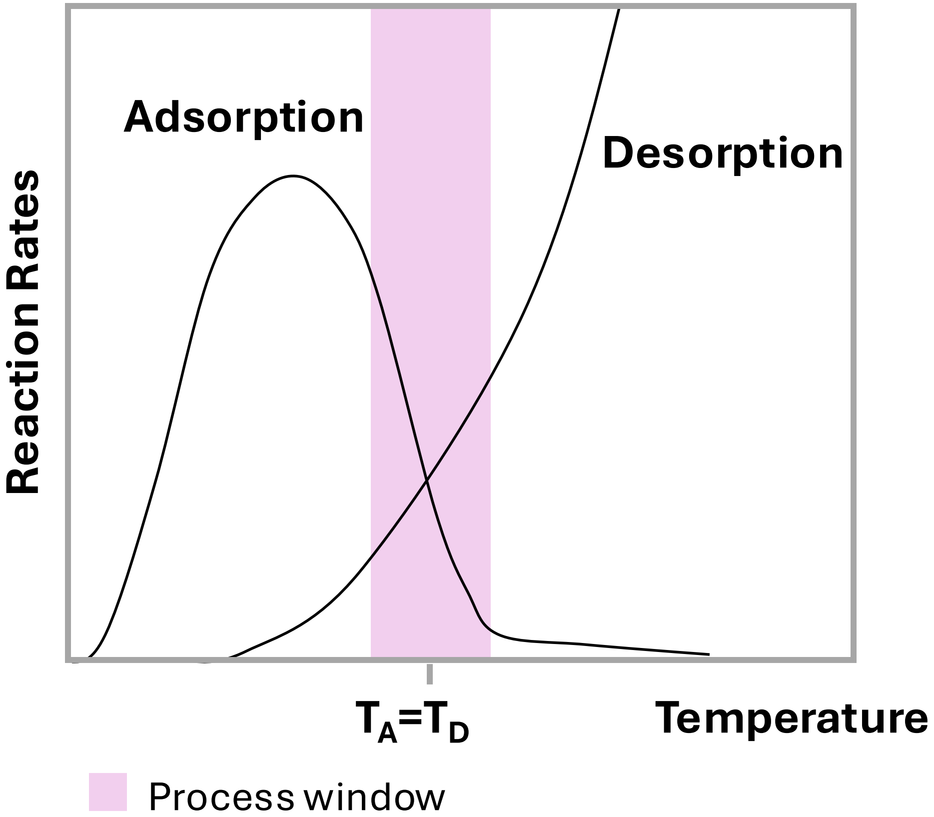


Bond energy conditions

Bond Energies	Fluorine	Chlorine	Bromine
E_A	5 .6 eV	4.7 eV	3.6 eV
E_S	0.9 eV	2.3 eV	>2.3 eV
E_O	4.7 eV		
 Condition for etching: $E_S < E_O$ and E_A	Etching 	Etching 	Desorption 

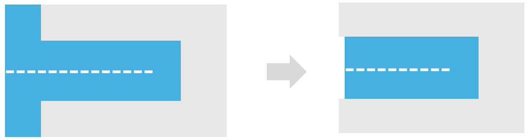
✂ = energy (kinetic energy, thermal energy, photons, etc.)

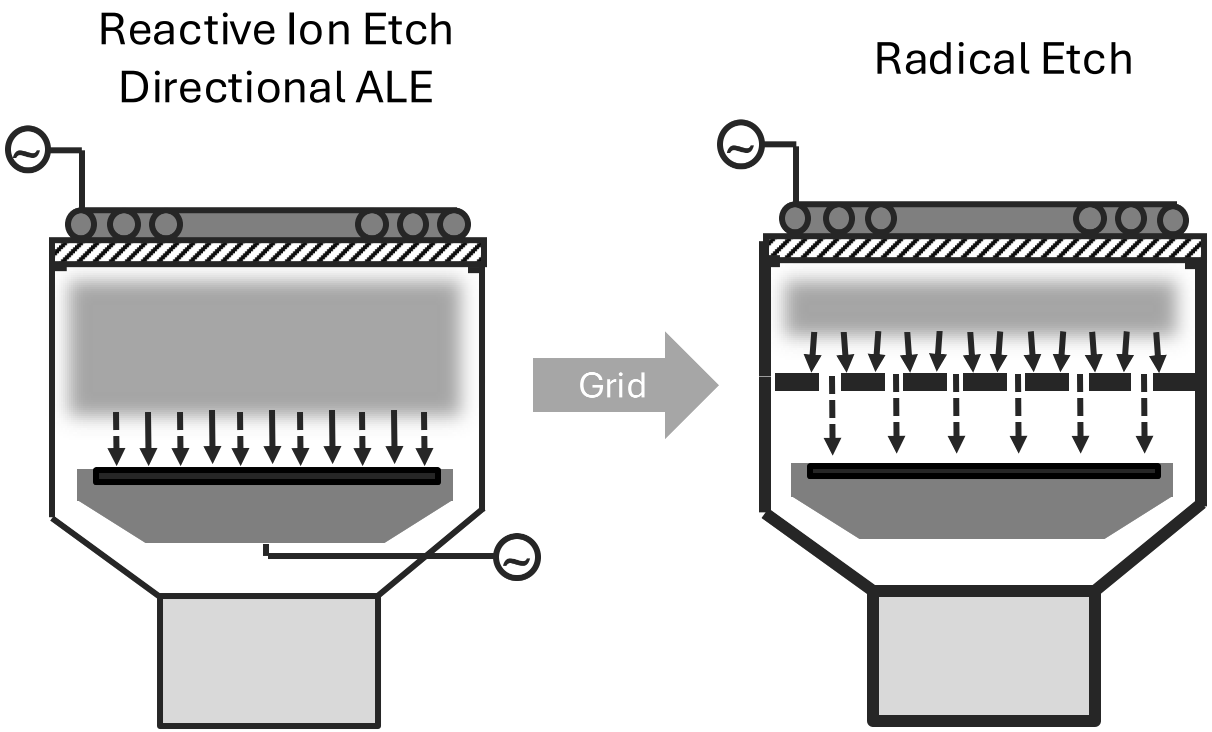
Example: Halogens on Si

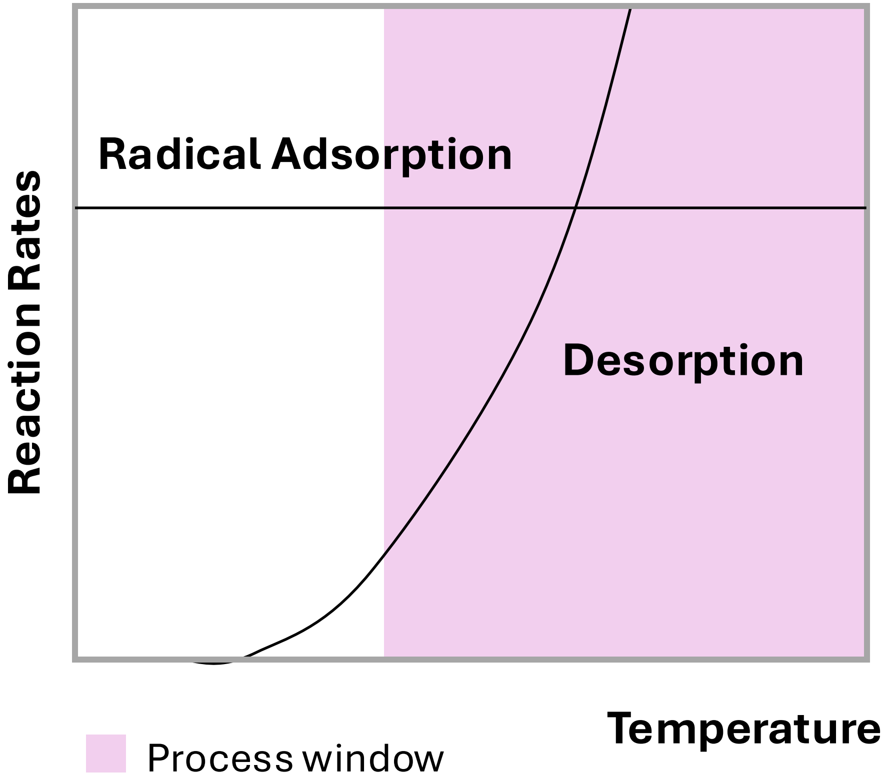


Process window does not exist for many material and gas combinations. It exists for metal oxides and halides in combination with various gases and in cases where the gas is fluorine based.

Selective Isotropic Etch: Radical Etch



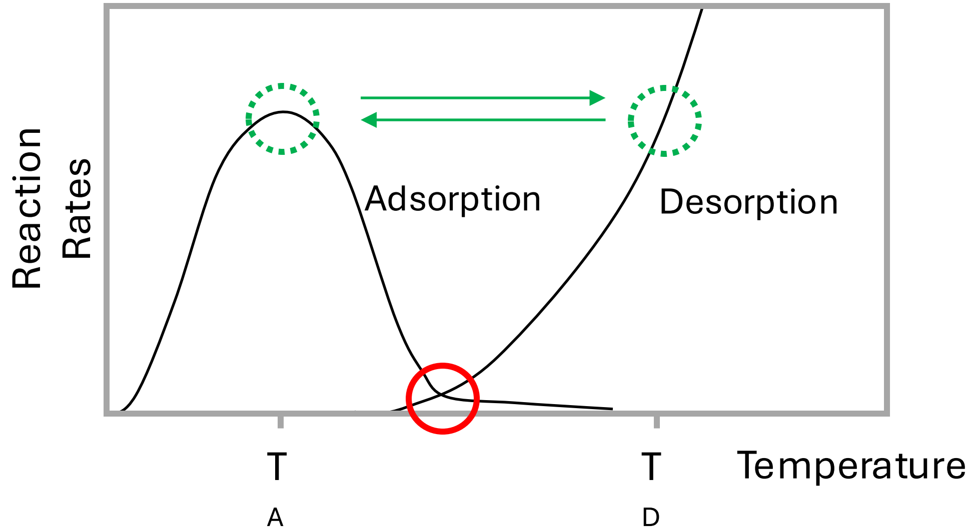




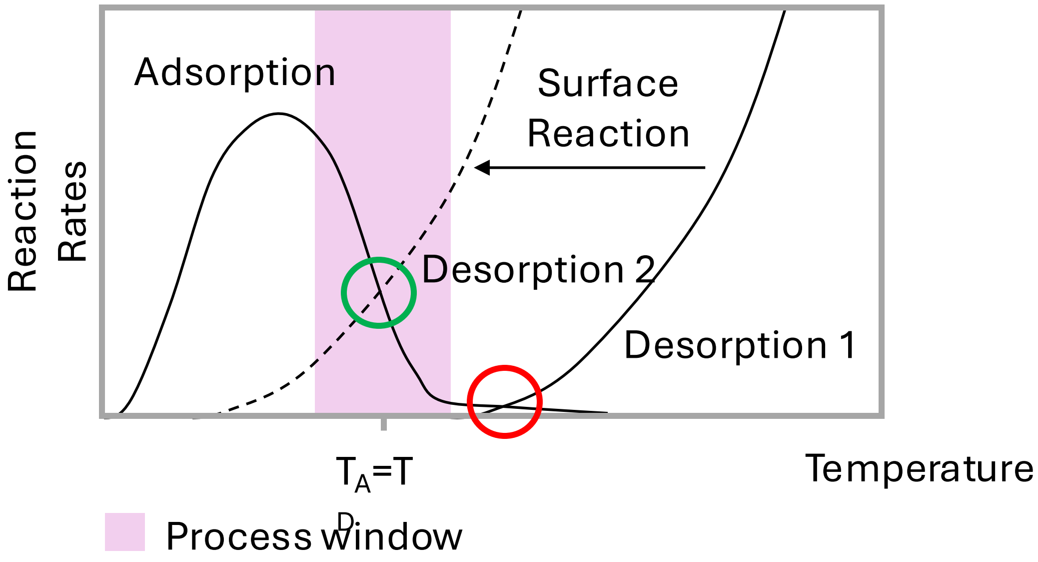
Radicals typically don't have a small energy barrier for chemical reactions. The adsorption process is therefore less temperature dependent than that of non-radical neutrals.

Selective Isotropic Etch: Thermal Atomic Layer Etch

Thermal ALE with Temperature Cycling

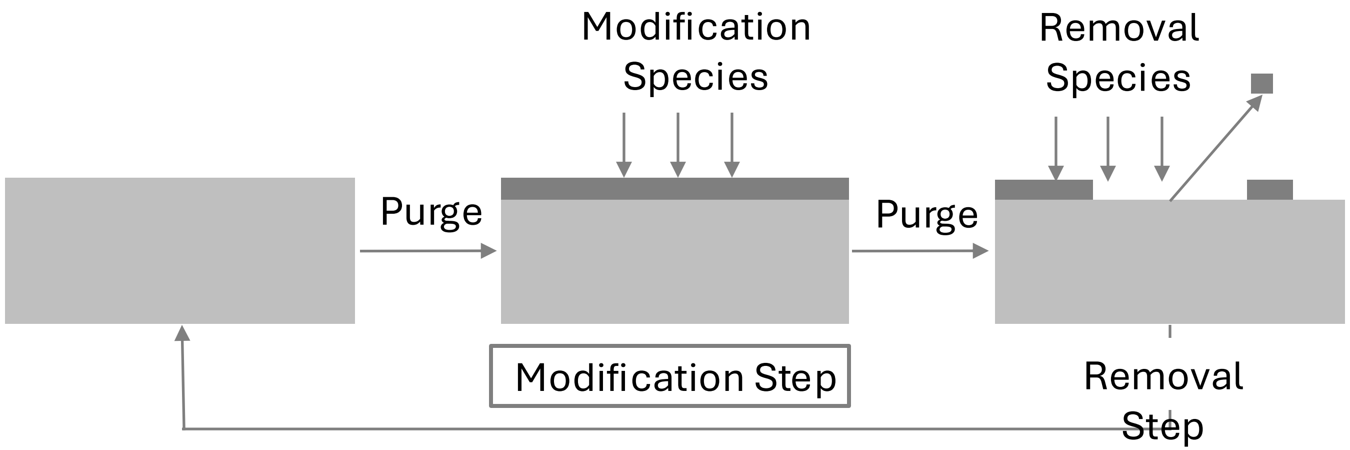


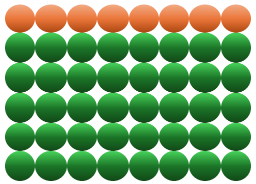
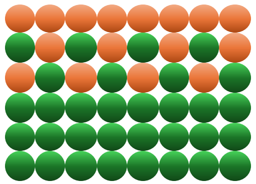
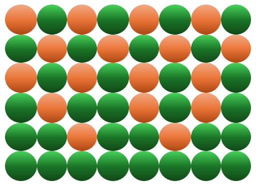
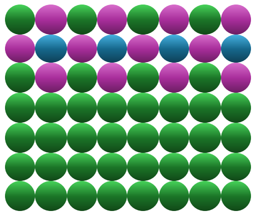
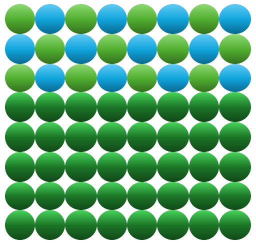
Thermal ALE with Ligand Exchange



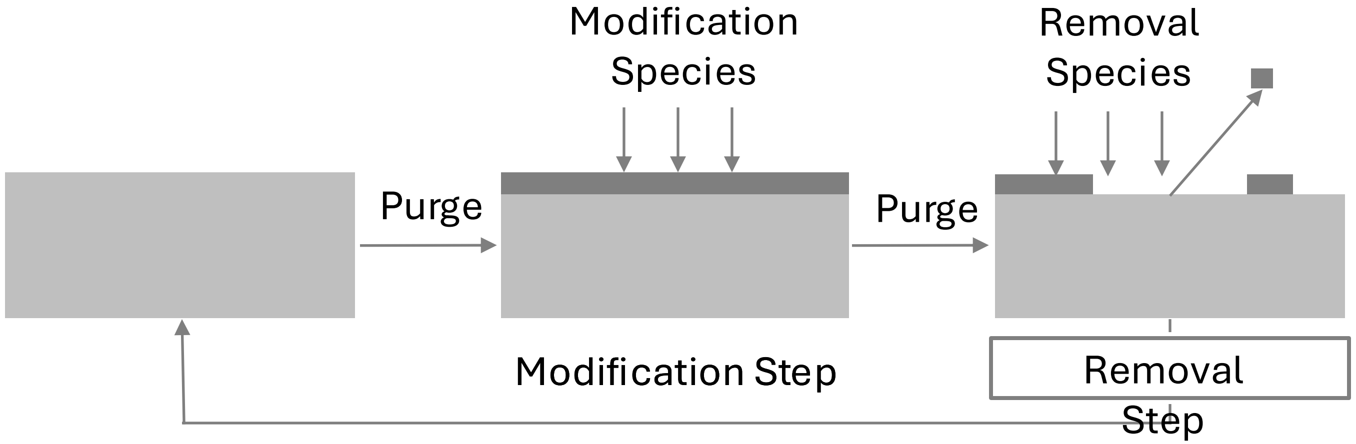
Lack of overlap of the adsorption and desorption process windows can overcome by temperature cycling or a second reaction.
The introduction of a second reaction divides process in modification and removal steps.

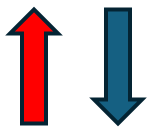
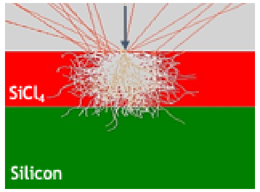
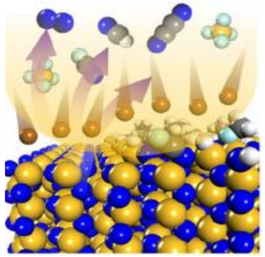
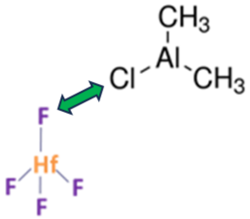
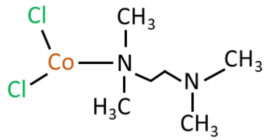
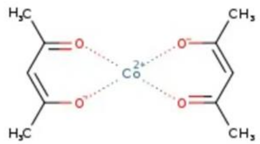
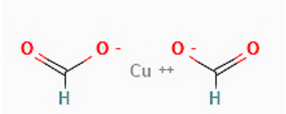
ALE Modification Step Types



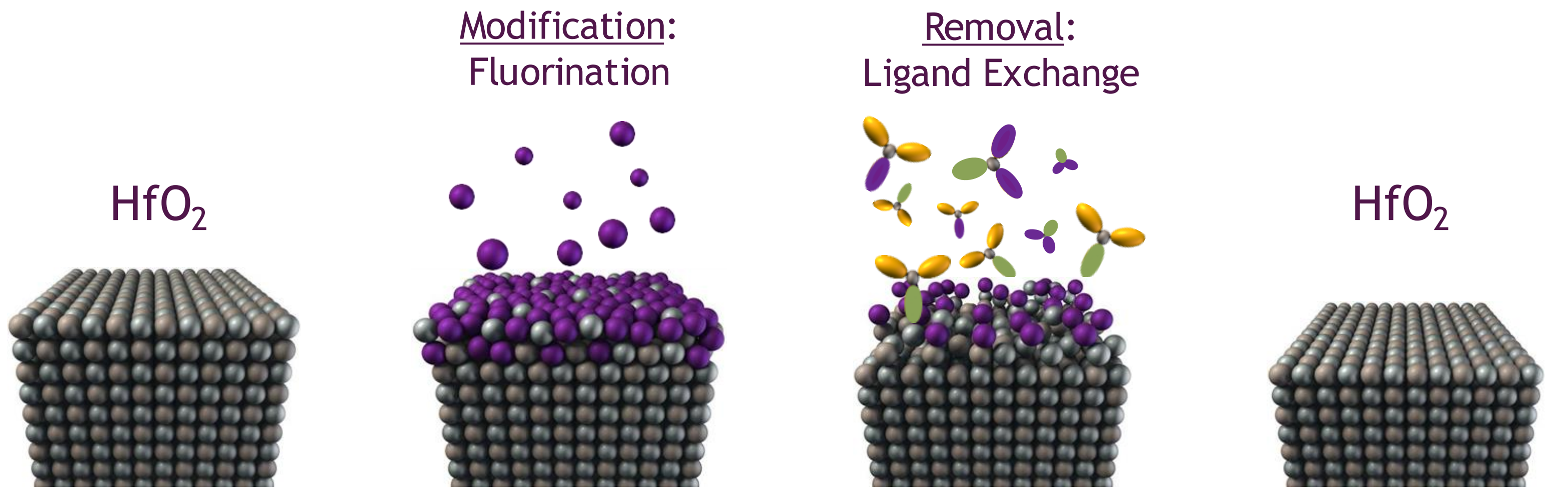
	Adsorption / Reaction	Adsorption / Diffusion / Reaction	Ion Implantation	Conversion	Deposition
					
Typical applications:	Plasma-less oxidation, fluorination, chlorination of metals, semiconductors, metal oxides	Plasma oxidation, fluorination, chlorination of metals, semiconductors, metal oxides	Plasma oxidation, nitridation, fluorination, chlorination of noble metals	Formation of $(NH_4)_2SiF_6$ on SiO_2 and SiN Conversion of SiO_2 into Al_2O_3	CFx on SiO_2, SiN BCl_x on metals and metal oxides

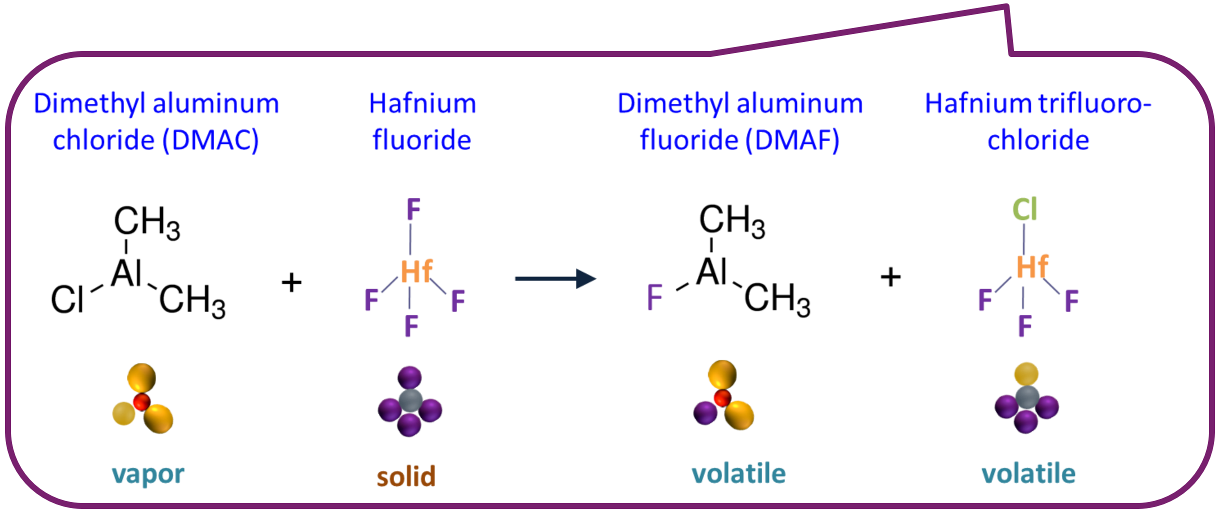
ALE Removal Step Types



	Thermal cycling	Ion bombardment	Remote Plasma	Ligand exchange	Ligand addition	Chelation	Organic Salts
	Temperature 						
Typical applications:	SiO_2 and SiN via Formation of $(NH_4)_2SiF_6$	Directional ALE of Si, Ge, dielectrics, metals, metal oxides	Selective SiGe Oxidation/fluorination and chlorination / fluorination of metals	Metal oxides and metals	Metal oxides and metals	Metal oxides and metals	Metal oxides and metals

Example of Thermal Isotropic ALE: HfO_2 HF/DMAC





Lee et al., Chem. Mater. **28**, 7657 (2016)

Proposed Ligand Exchange Reactions

<u>ALE cycle:</u>

Fluorination: $4\ HF + HfO_2 \rightarrow HfF_4 + 2\ H_2O$

Ligand Exchange: $AlCl(CH_3)_2 + HfF_4 \rightarrow AlF(CH_3)_2 + HfF_3Cl$

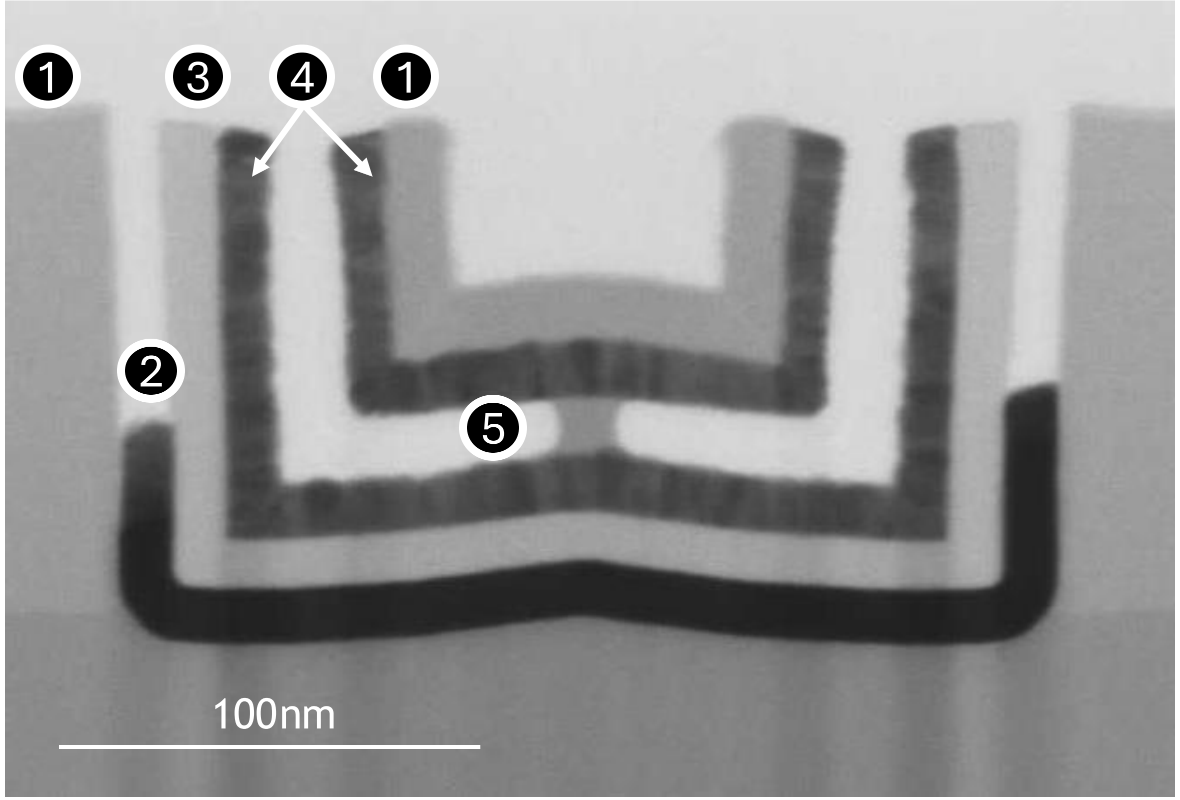
Reaction may repeat until $HfCl_4$ is formed.

HfF_4 boiling point: 970 ℃

$HfCl_4$ sublimes at: 317 ℃

Thermal ALE can achieve good ARDE.

Etch amount of Thermal Isotropic ALE with HF/DMAC for various materials

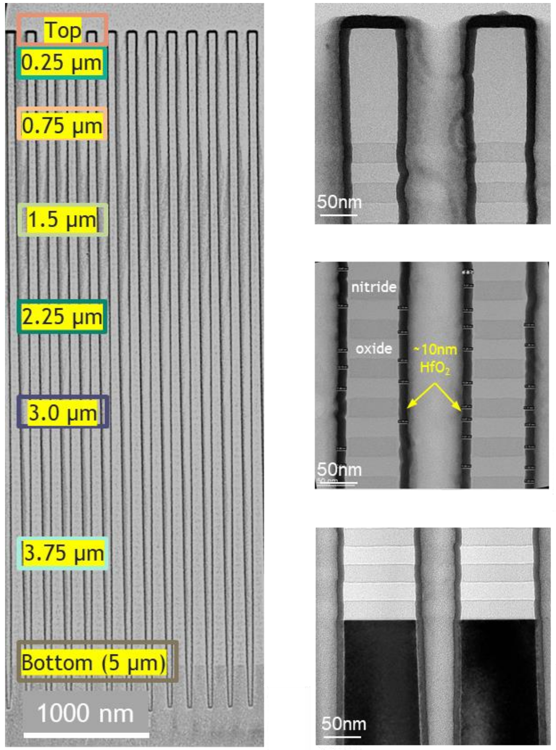


	Material	Etch Amount / nm
1	SiN	Not measurable
2	HfO_2	62.3
3	SiO_2	Not measurable
4	TiN	Not measurable
5	Al_2O_3	111.6

A. Fischer, T. Lill, Phys. Plasmas 30, 080601 (2023).

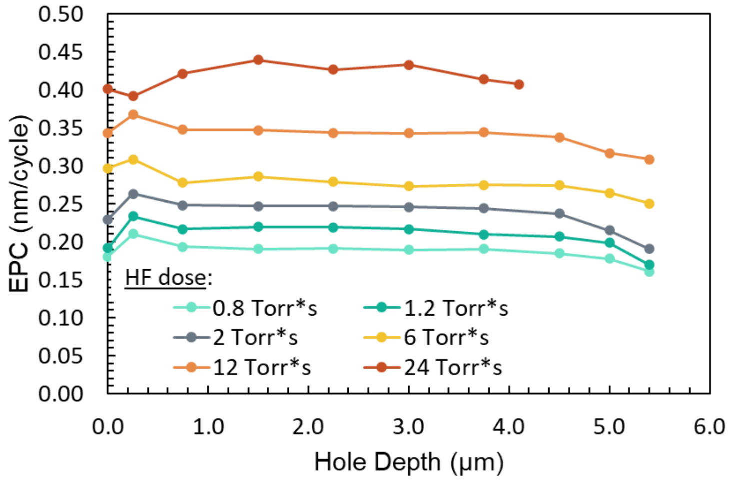
Thermal ALE enables isotropic selective etching of many “hard to etch” materials.

Thermal Isotropic Atomic Layer Etching: Aspect Ratio Dependence



Example:
HfO_2 thermal ALE with HF/DMAC, variable gas dose

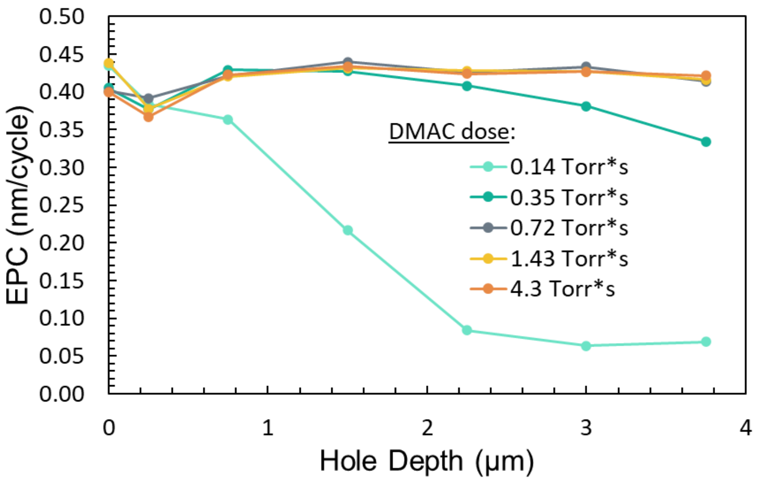
Fluorination



$HfO_2 + 4\,HF \rightarrow HfF_4 + 2\,H_2O$

- **Fluorination with HF:**
- Etch rate is affected by HF dose
- Cause: low reactivity but high mobility of HF molecules on HfO_2 surfaces

Ligand exchange



$HfF_4 + AlCl(CH_3)_2 \rightarrow HfF_3Cl + AlF(CH_3)_2$

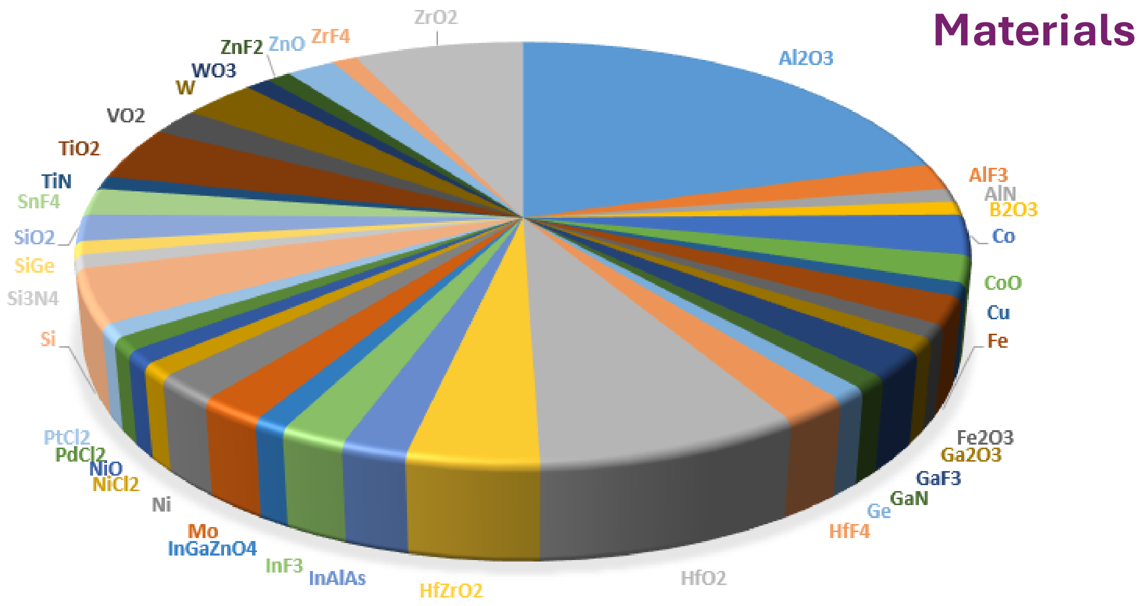
- **Ligand exchange with DMAC:**
- ARDE is affected by DMAC dose
- Cause: high reactivity but low mobility of DMAC molecules on fluorinated HfO_2 surfaces

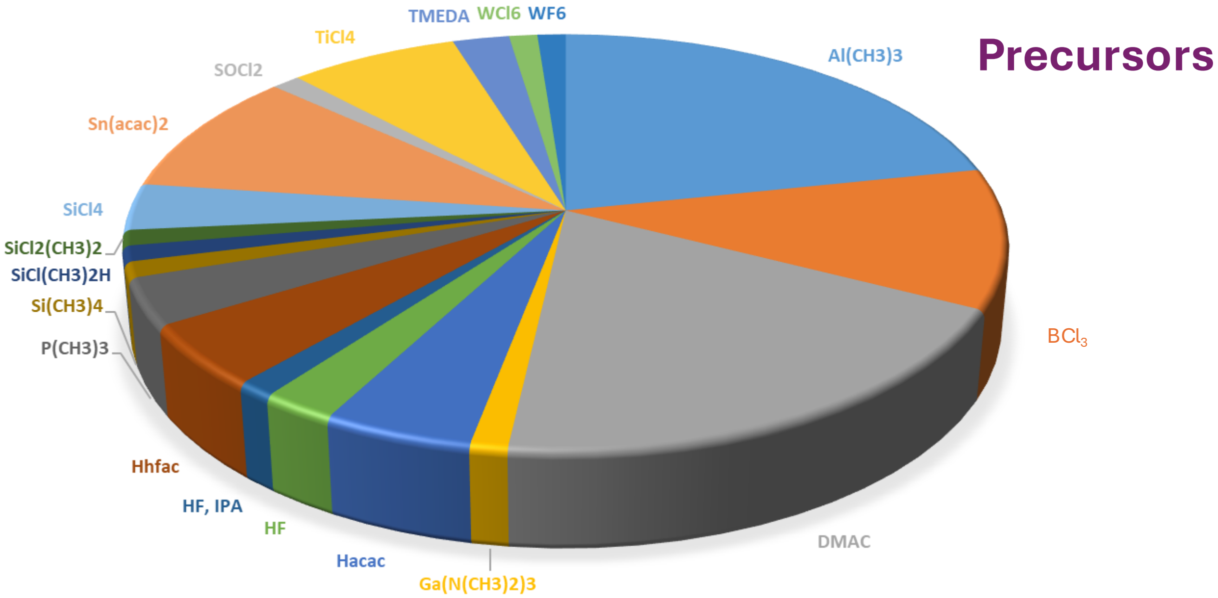
Thermal ALE can achieve good ARDE.

Materials and Precursors

Material type	Precursors	Conversion to
Metals		
Co	H^+hfac, H^+acac	chloride
Cu, Ni	H^+hfac	oxide
Fe	H^+acac	chloride
Ge	thermal cycling	chloride
Mo, W	BCl_3	oxide then B_2O_3
Ni, Pd, Pt	$P(CH_3)_3$	chloride
Metal oxides		
Ga_2O_3, VO_2, ZnO, $InGaZnO_4$,	$Al(CH_3)_3$, DMAC,	fluoride
Al_2O_3, $HfSiO_2$, HfO_2, $HfZrO_2$, ZrO_2	$Sn(acac)_2$	fluoride
CoO, ZnO, F_2O_3, NiO	TMEDA	chloride
Nitrides		
AlN	$Sn(acac)_2$	fluoride
GaN	BCl_3	fluoride
Si_3N_4	$Al(CH_3)_3$	Al_2O_3
TiN	HF	oxide
Semiconductors		
InAlAs, InGaAs	DMAC	fluoride
Si	BCl_3	oxide then B_2O_3
Oxides		
SiO_2	$Al(CH_3)_3$	fluoride
$InGaZnO_4$	DMAC	fluoride

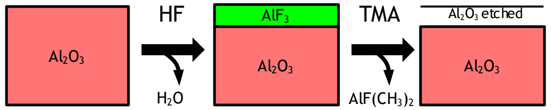
Source: A. Fischer, SPIE short course





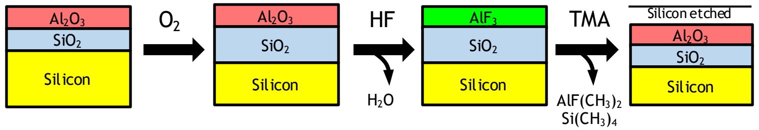
Mechanisms and types of Thermal Isotropic ALE

Ligand exchange (example: Al_2O_3)



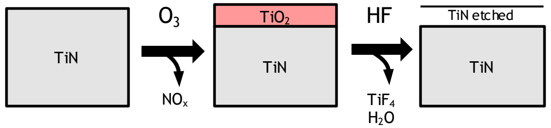
Y. Lee *et al.*,
Chem. Mater. **28**, 9, 2994 (2016)

Conversion (example: silicon)



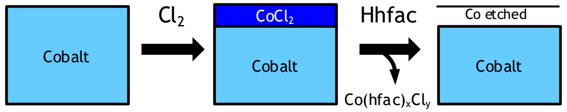
A.I. Abdulagatov *et al.*,
Chem. Mater. **30**, 8465 (2018)

Oxidation / Fluorination (example: TiN)



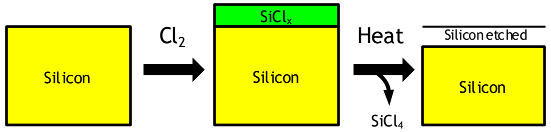
Y. Lee *et al.*,
Chem. Mater. **29**, 19, 8202 (2017)

Chelation with diketones (example: cobalt)



M. Konh *et al.*,
J. Vac. Sci. Technol. A **37**, 021004 (2019)

Conversion and thermal cycling (example: silicon)



S. Imai *et al.*,
Jpn. J. Appl. Phys. **34,** 5049 (1995)

Fluorination and ligand-exchange. The first example was published by Lee et al. on Al_2O_3 ALE using HF and $Sn(acac)_2$.

Oxidation, conversion, fluorination and ligand-exchange. This is an ALE mechanism that is particularly relevant for silicon ALE. Elemental silicon is oxidized either at high temperature with O_2 or with O_3. Its oxide is then converted into aluminum oxide via TMA and the latter volatilized using ligand-exchange with TMA.

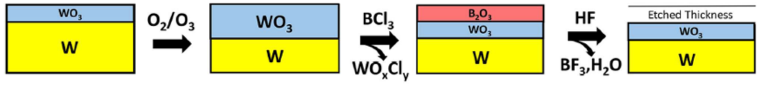
Oxidation to raise the oxidation state. This approach has been used if a lower oxidation state of a metal is not reactive with a compound that volatilizes it, but the higher oxidation state is. In TiN, for example, the oxidation state of the metal can be increased from 3+ when it is bonded to nitrogen to 4+ via oxidation with ozone to TiO_2.

Halogenation followed by reaction with diketons. A cobalt ALE process exists which uses chlorine to modify the surface and hexafluoro-acetylacetone or acetylacetone in the removal step.

Temperature modulation mechanism. Ikeda et al. (Appl. Surf. Sci. 112, 87 (1997)) proposed an ALE mechanism for metallic germanium during which its surface is modulated with chlorine at lower temperatures and then volatilized at a higher temperature.

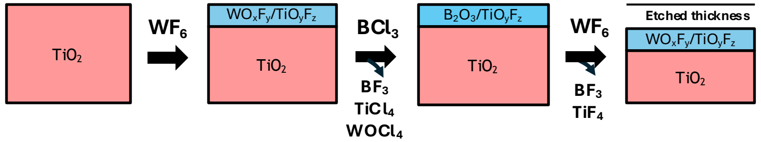
Mechanisms and types of Thermal Isotropic ALE

Oxidation, conversion and volatile fluoride (example: tungsten)



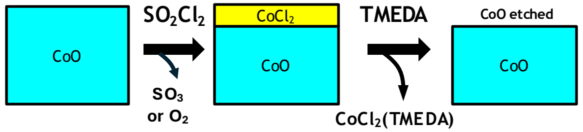
Johnson *et al.*, ACS Appl. Mater. Interfaces 9, 34435 (2017)

Chlorine-fluorine exchange (example: titanium oxide)



Lemaire *et al.*, Chem. Mater. 29, 16, 6653 (2017)

Ligand addition (example: cobalt oxide)



Partridge *et al.*, Chem. Mater. 35, 2058 (2023)

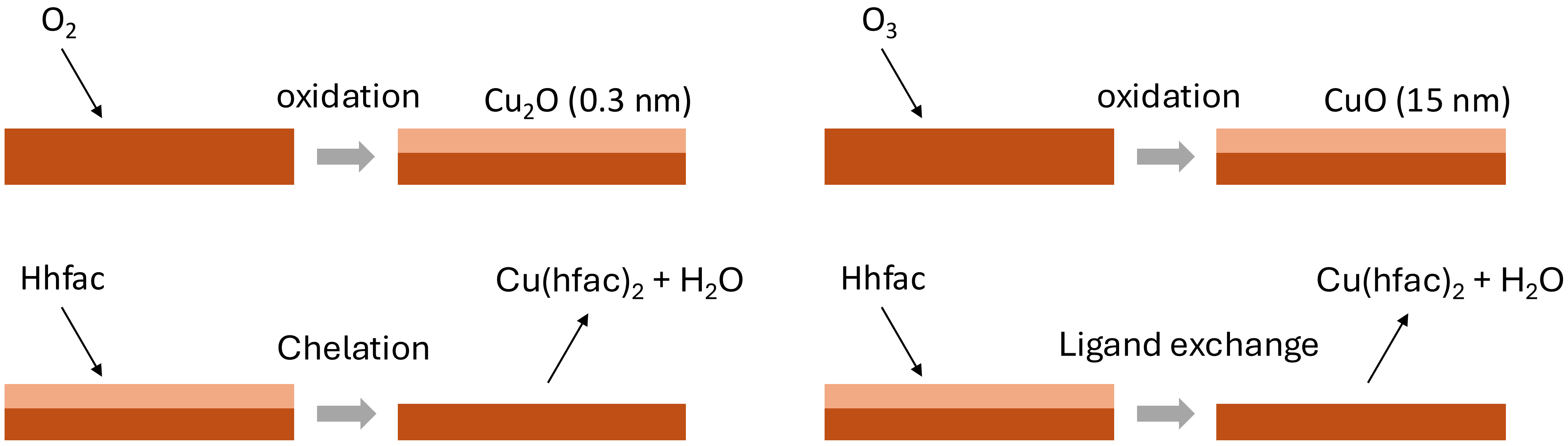
<u>Oxidation, conversion to another metal oxide and fluorination to volatile fluoride.</u> This class has been reported for etching of tungsten or molybdenum, respectively. The conversion to another metal oxide such as B_2O_3 is preceded by a primary oxidation of the metal via O_3 or an O_2 plasma.

<u>Chlorine-fluorine ligand-exchange.</u> For example, TiO_2 can be fluorinated via WF_6 at lower temperatures (<170°C) and its fluorine ligands replaced by chlorine via application of BCl_3 resulting in a volatilization of titanium.

<u>Ligand addition.</u> Lii-Rosales et al., Partridge et al., and Murdzek et al. showed that metals such as Ni, Pd, Pt and metal oxides such as CoO, ZnO, Fe_2O_3, and NiO can be etched after chlorination using TMEDA (Tetramethylethylenediamine) and trimethylphosphine.

Several mechanisms for thermal ALE have been discovered.
The most versatile are ligand exchange, ligand addition chelation, and oxidation/fluorination.

Thermal ALE of "hard to etch" materials": Copper



$Cu_2O + 2Hhfac = Cu(hfac)_2 + Cu + H_2O$

$CuO + 2Hhfac = Cu(hfac)_2 + H_2O$

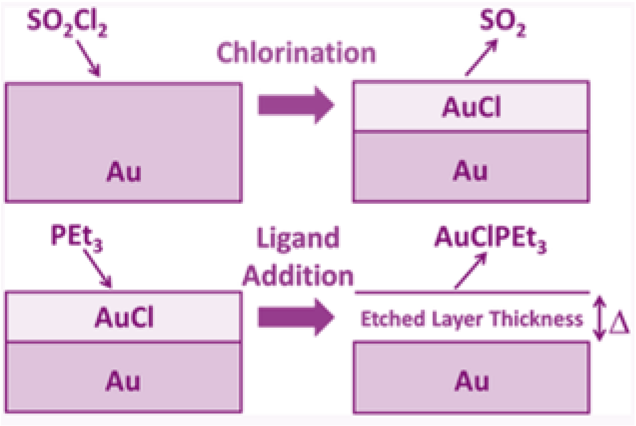
Increase in surface roughness

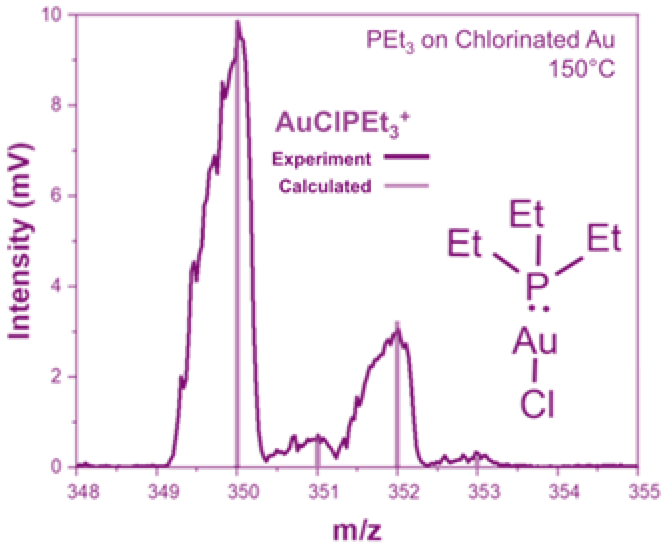
No change in surface roughness

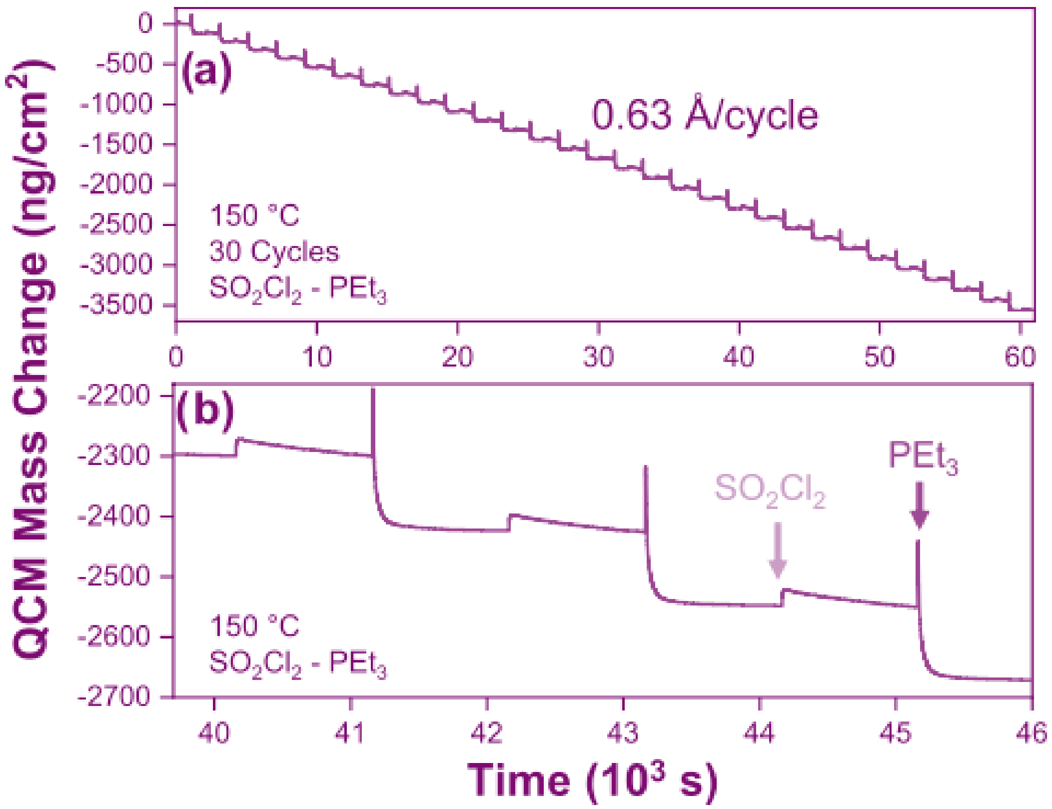
E. Mohimi, X. Chu, B. Trinh, S. Babar, G. Girolami, J. R. Abelson, "Thermal Atomic Layer Etching of Copper by Sequential Steps Involving Oxidation and Exposure to Hexafluoroacetylacetone", ECS Journal of Solid State Science and Technology **7**, P491 (2018).

Copper can be etched using chelation reaction with copper oxide.

Thermal ALE of “hard to etch” materials”: Gold



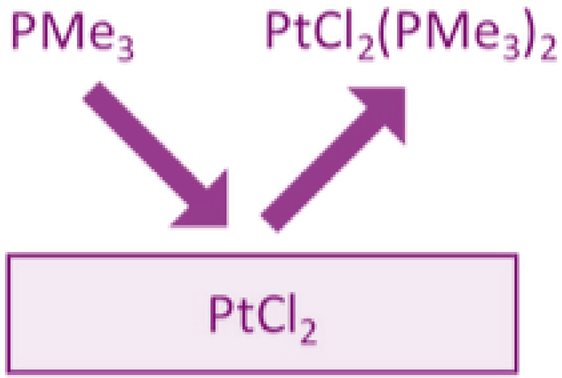


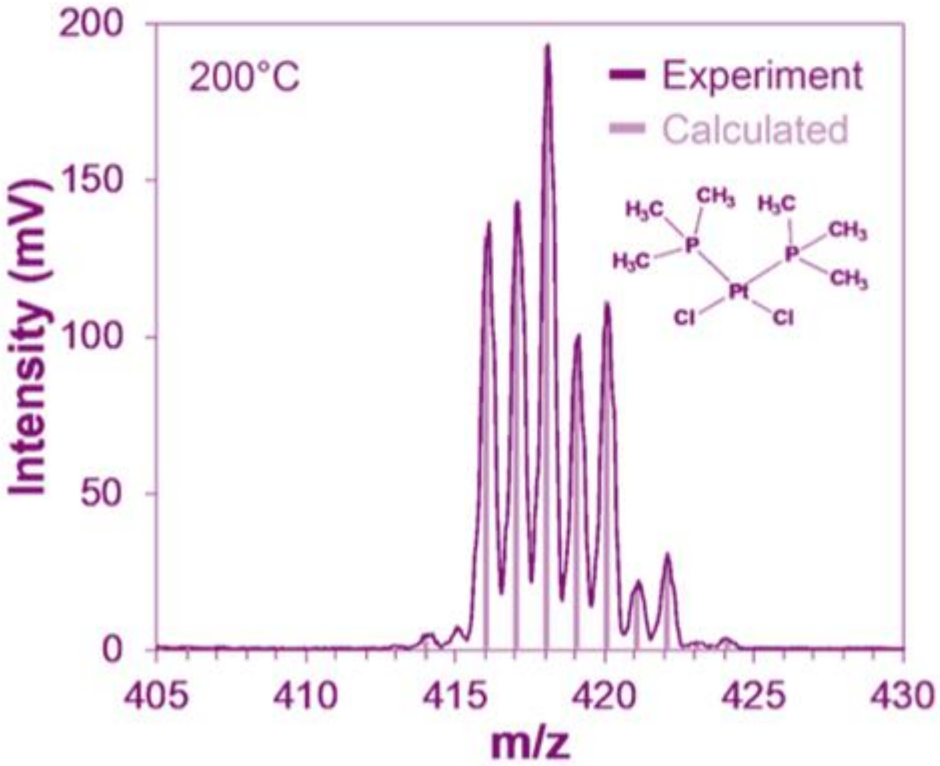


J. Partridge, J. Murdzek, V. Johnson, A. Cavanagh, V. Sharma, S. M. George, “Thermal Atomic Layer Etching of Gold Using Sulfuryl Chloride for Chlorination and Triethylphosphine for Ligand Addition”, Chem. Mater. **36**, 5149 (2024).

Gold can be etched with thermal ALE using SO_2Cl_2 sulfuryl chloride and $P(Me)_3$ as the reactants using a ligand addition mechanism.

Thermal ALE of “hard to etch” materials”: Platinum





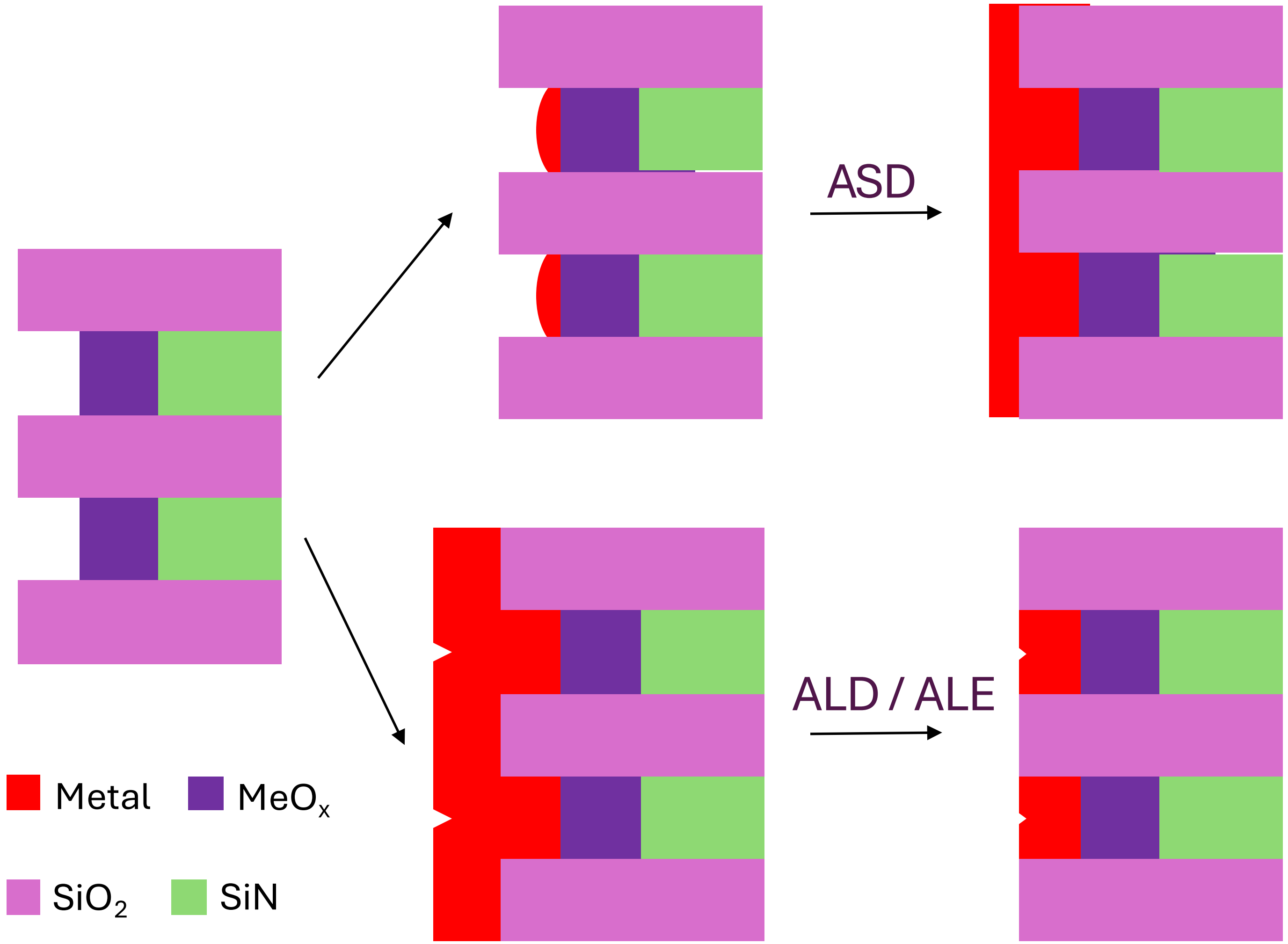
A. Lii-Rosales, V. L. Johnson, S. Sharma, A. Fischer, T. Lill, S. M George, “Volatile Products from Ligand Addition of $P(CH_3)_3$ to $NiCl_2$, $PdCl_2$, and $PtCl_2$: Pathway for Metal Thermal Atomic Layer Etching”, J. Phys. Chem. C **126**, 8287 (2022).

Trimethylphosphine etches $PtCl_2$ via ligand addition mechanism. This suggests that Pt thermal ALE should be possible using SO_2Cl_2 and $P(Me)_3$ as the reactants.

Performance Metrics: Radical Etch vs. Thermal Etch and Thermal ALE

Metric	Thermal Etch	Thermal ALE	Radical etch	Explanation
Materials Versatility				Based on the number of known etching chemistries.
Etch rate				Cycling in ALE limits etching rate.
Uniformity across wafer				Thermal and radical etch require gas flow tuning across wafer.
Aspect Ratio Dependent Etching (ARDE)				Recombination of radicals on sidewalls.
Surface smoothness				Thermal etch: Very sensitive to crystalline structure and composition changes.
Selectivity				Radical etch: Chemical contrast reduced by radical reactivity.
CD control				ALE is superior due to self-limited steps.

Main Challengs for ASD and ALD / Selective Isotropic Etch

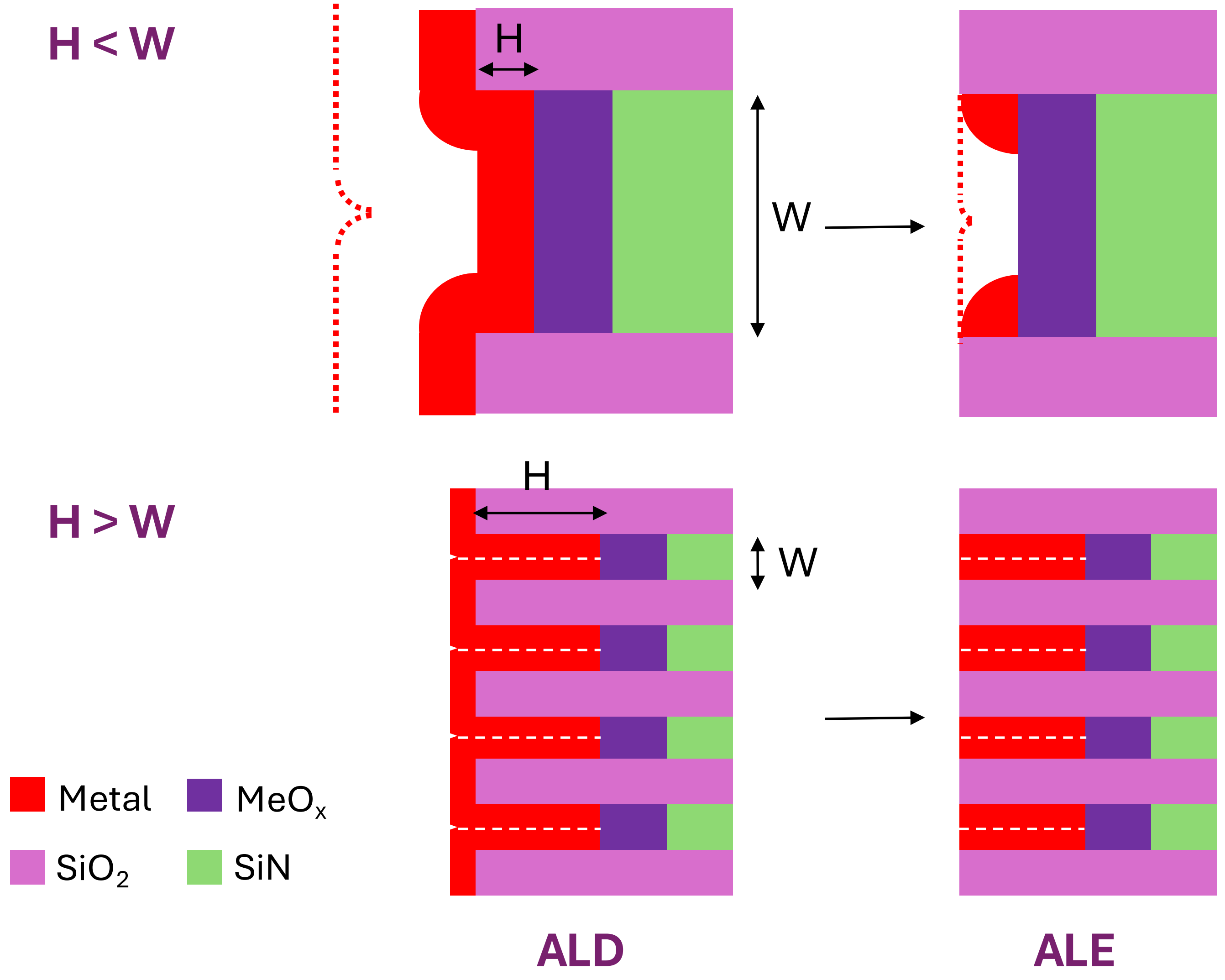


- **Selectivity to dielectric isolation layer**
- Selectivity enhancement steps maybe needed (ALE etchback, blocking layers)
- Very long deposition for fill of deep recesses

- **ALE sensitivity to voids**
- Longer process due to ALE etchback
- Process time depth independent
- Halogen residues after ALE
- Very long etch for thin layers in deep recesses

ASD is very challenging, and processes are not widely available.
ALD / ALE film stacking can be applied to film stacking in narrow and deep structures.

Aspect Ratio Dependence of ALD / Selective Isotropic Etch Film Stacking

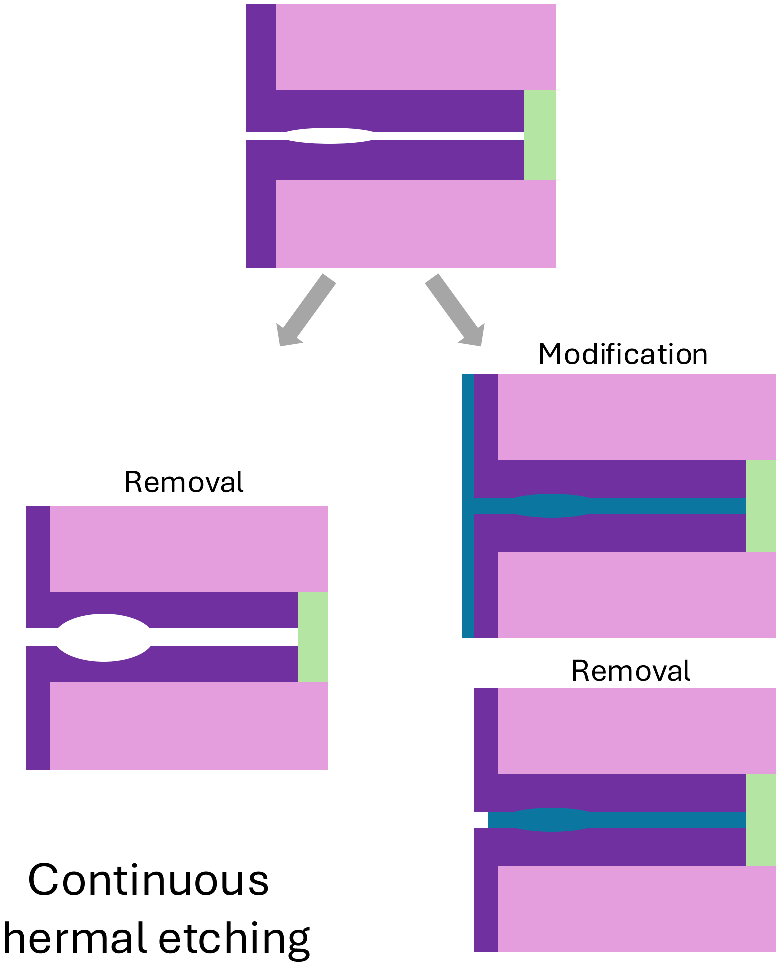


- For aspect ratios H/W < 1, material insertion with ALD / ALE requires large overburden
- This increases cost and space may not be available
- **Bottoms-up area selective ALD (ASD) is preferred**

- For aspect ratios H/W < 1, ALD / ALE materials insertion is feasible and efficient
- Throughout for ALD and ALE is proportional to W only
- **ALD / ALE insertion is preferred**

ALD / ALE film stacking can be applied to film stacking in narrow and deep structures.

Seam / Void Sensitivity of ALD/ALE Integration

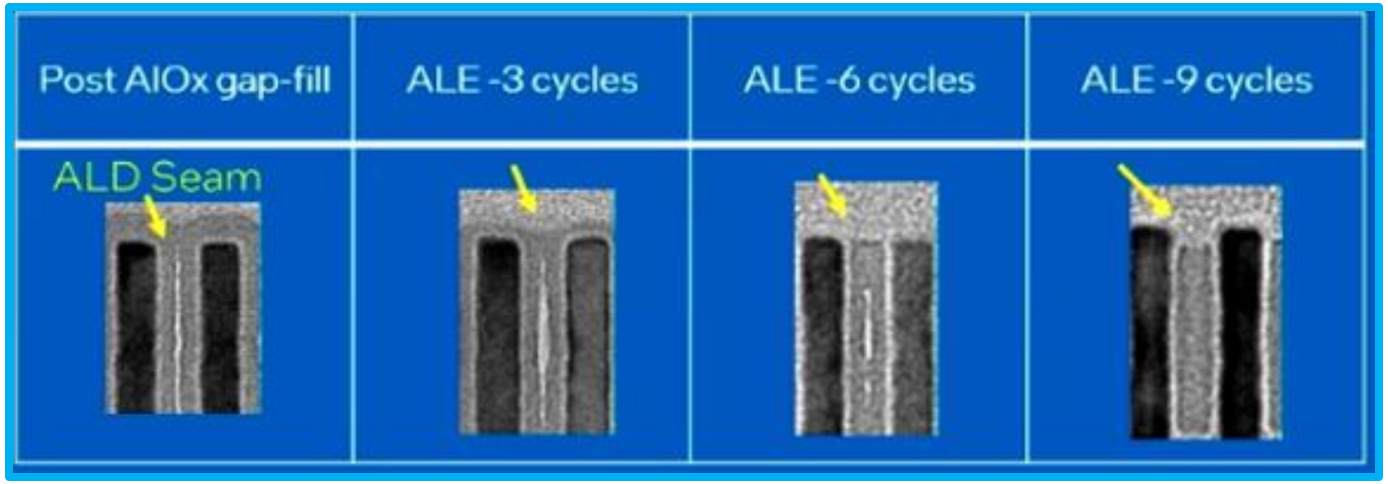


Continuous thermal etching

Thermal ALE with volume expansion during modification

Al_2O_3 AlF_3

SiO_2 SiN

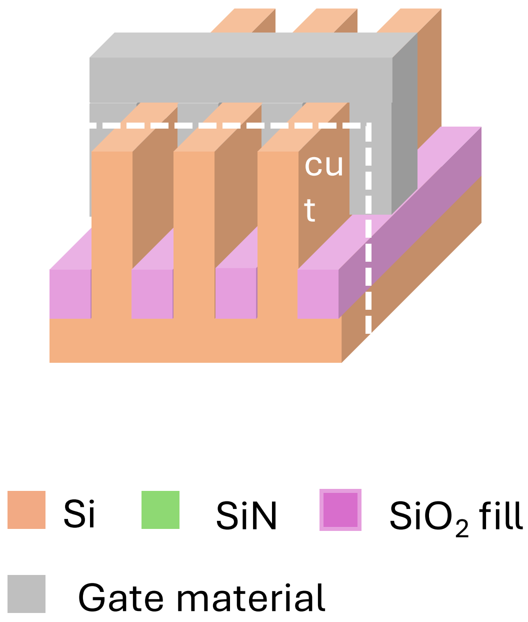


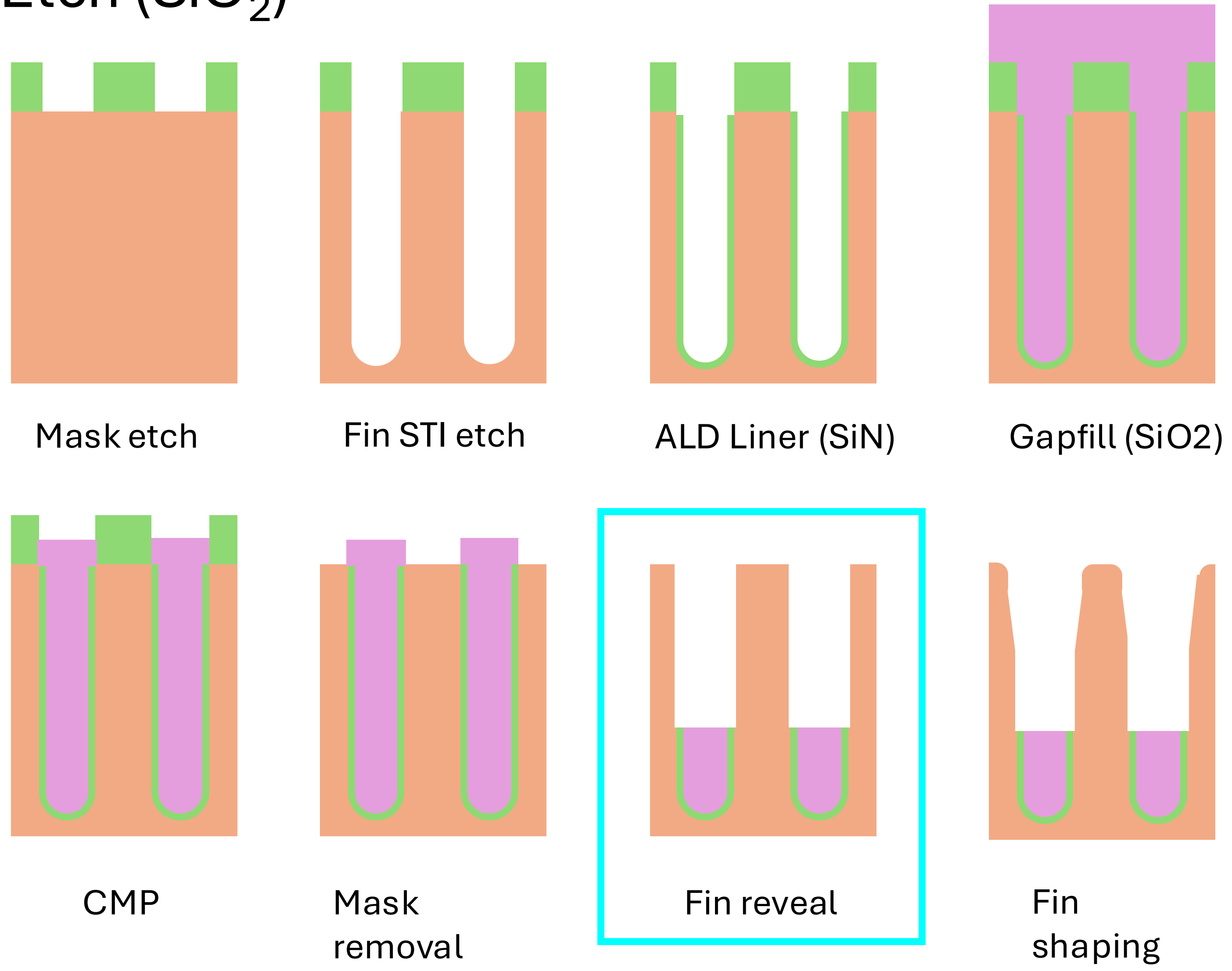
ALE of Al_2O_3 with fluorine / RCl_x

D. Kioussis, ALD/ALE conference 2024

Void attack can be prevented in ALE if the molar volume of the modified film is larger than of the original film.

Logic Devices: Fin Reveal Etch (SiO_2)





Fin reveal is one of the critical isotropic etch applications in FinFET gate integration.

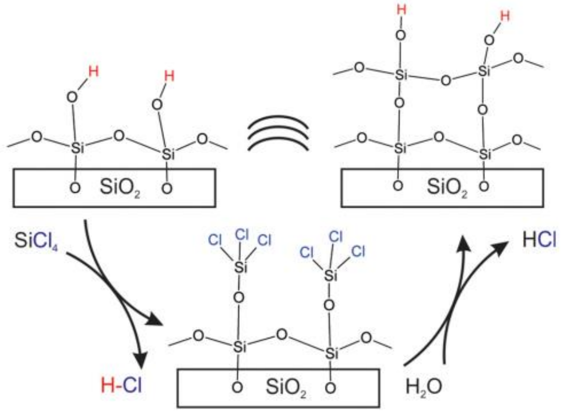
ALD of SiO_2 and SiN

SiO_2

Thermal ALD (room temperature):

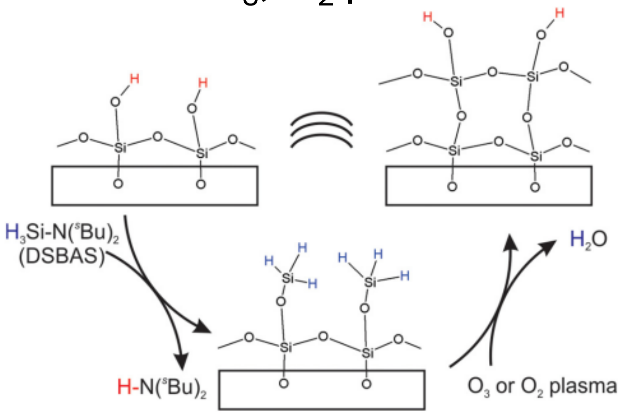
$SiCl_4$ / H_2O with pyridine or NH_3 catalysts (RT)

Tetraethoxysilane (TEOS) / H_2 with NH_3 catalyst (RT)



PEALD:

Aminosilanes / O_3, O_2 plasma



SiN

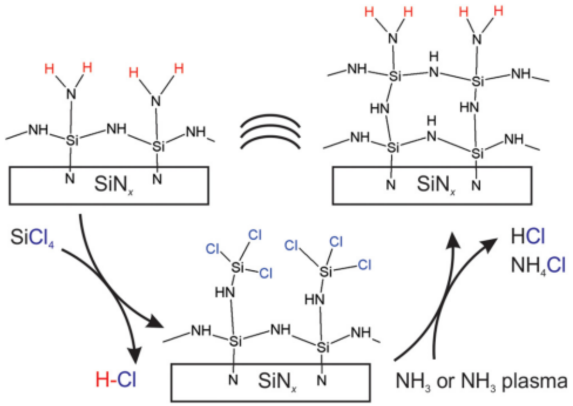
Thermal ALD:

$SiCl_4$ / NH_3 (>400℃)

PEALD:

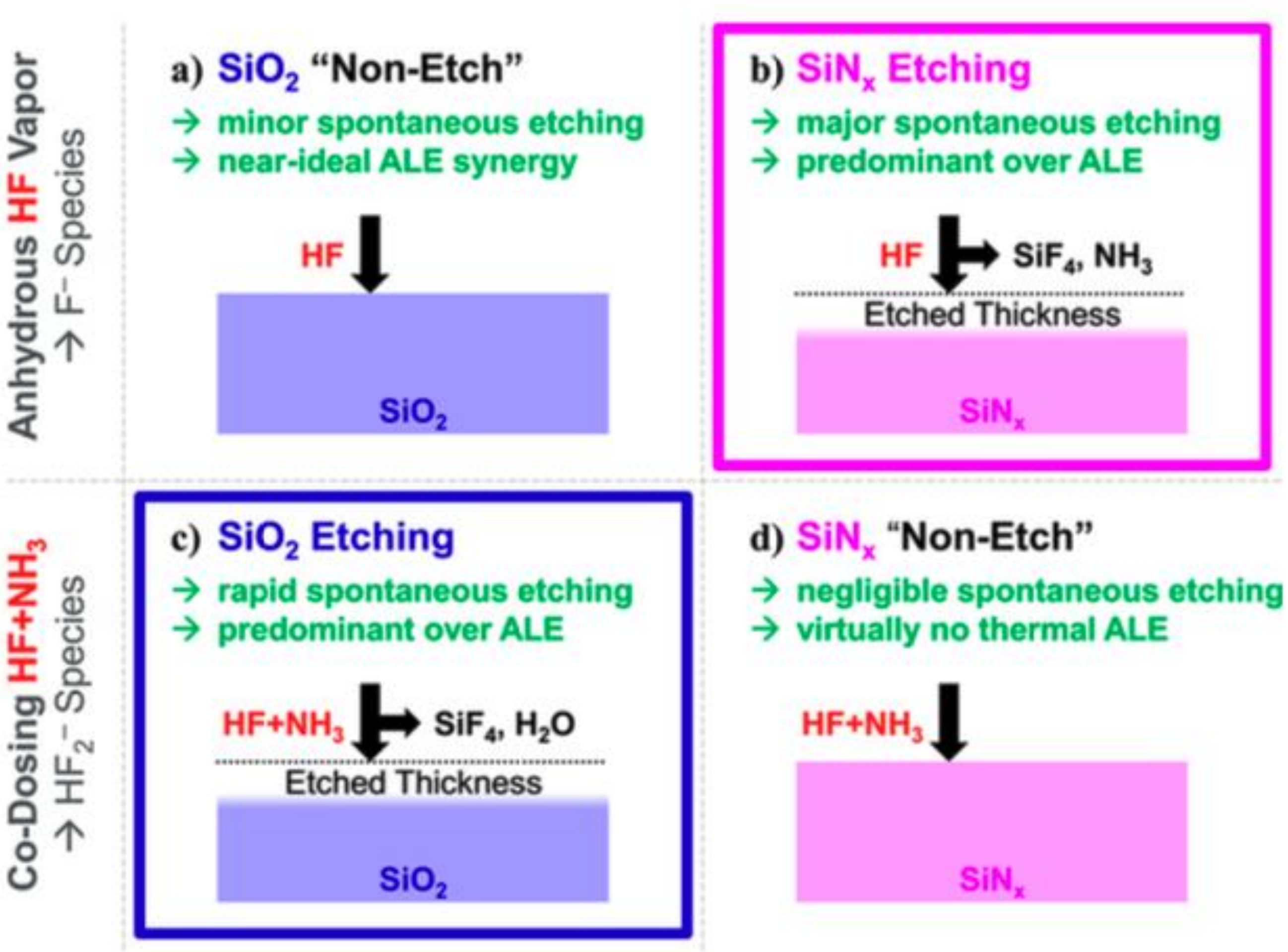
SiH_2Cl_2 / NH_3 plasma (250-400℃)

BTBAS / N_2 (80 – 500 ℃)



Ovanesyan et al. J. Vac. Sci. Technol. A 37, 060904 (2019).

Thermal Etching / ALE of SiO_2 and SiN with HF and NH_3



HF and NH_3 gases can etch SiO_2 and SiN with high selectivity with respect to each other.
To improve ARDE, the gases can be cycled (imec, TEL, SPIE 2022).

These processes may involve the formation of $(NH_4)2SiF_6$ (opinion of presenter, not mentioned in paper).

$$SiO_2 + 6HF + 2NH_3 \longrightarrow (NH_4)_2SiF_6 + 2H_2O$$

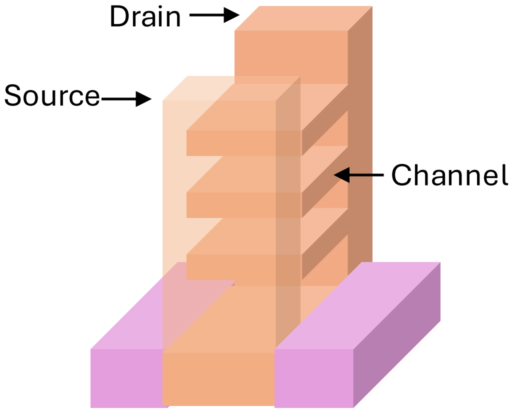
$$Si_3N_4 + 16HF \longrightarrow 2(NH_4)_2SiF_6 + SiF_4$$

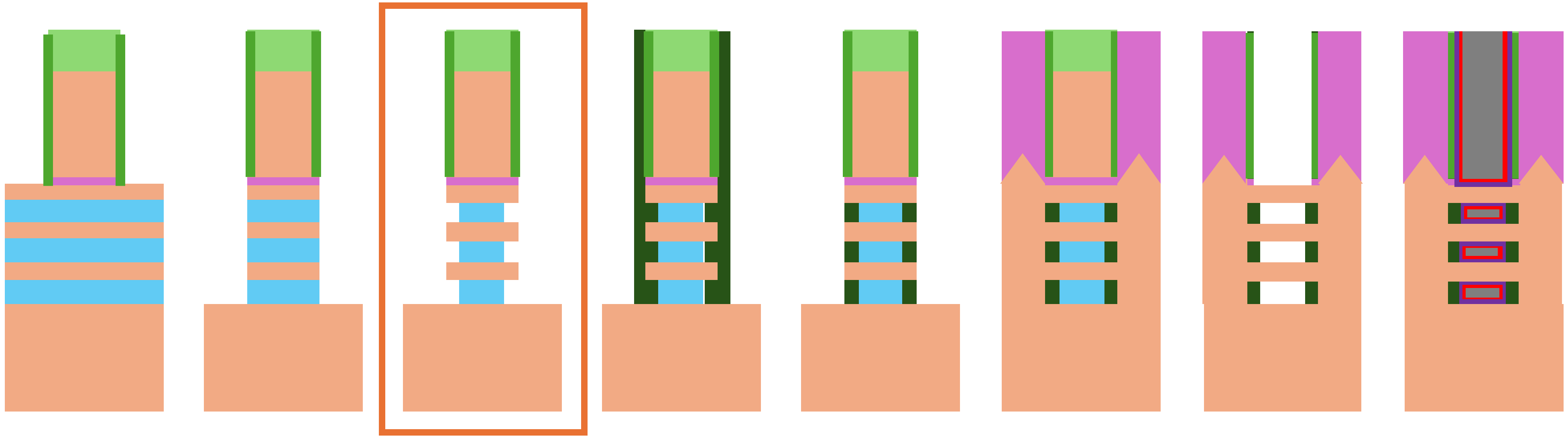
$$(NH_4)_2SiF_6 \xrightarrow{heat} 2NH_3 + SiF_4 + 2\,HF$$

M. Junige, S. M. George, "Selectivity between SiO_2 and SiN_x during Thermal Atomic Layer Etching Using $Al(CH_3)_3$/HF and Spontaneous Etching Using HF and Effect of HF + NH_3 Codosing",

Logic Devices: Nanosheet Cavity Etch (Si/SiGe)

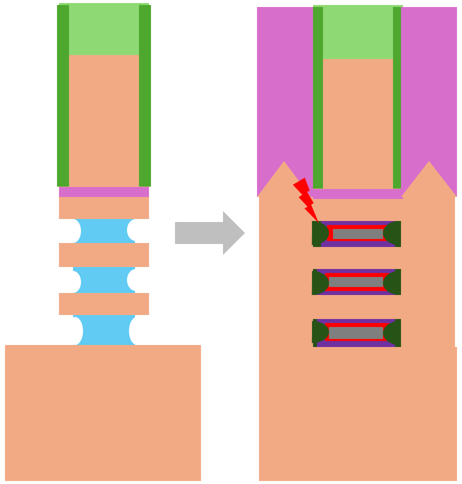
Target structure:





Requirements:

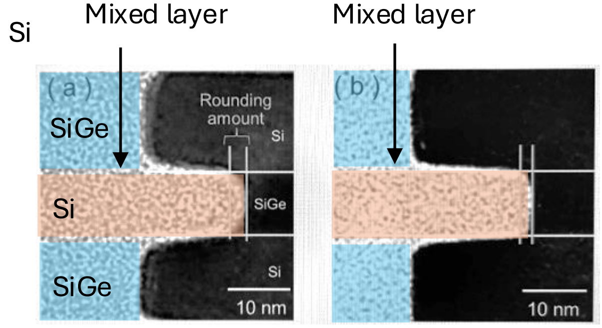
- Infinite selectivity SiGe / Si and in the future SiGe (1) / SiGe (2)
- Ge concentration as low as possible to avoid lattice defects and interface diffusion
- Square etch front
- Square tip



Rounded etch front leads to leakage between source / drain and channel

Solutions:

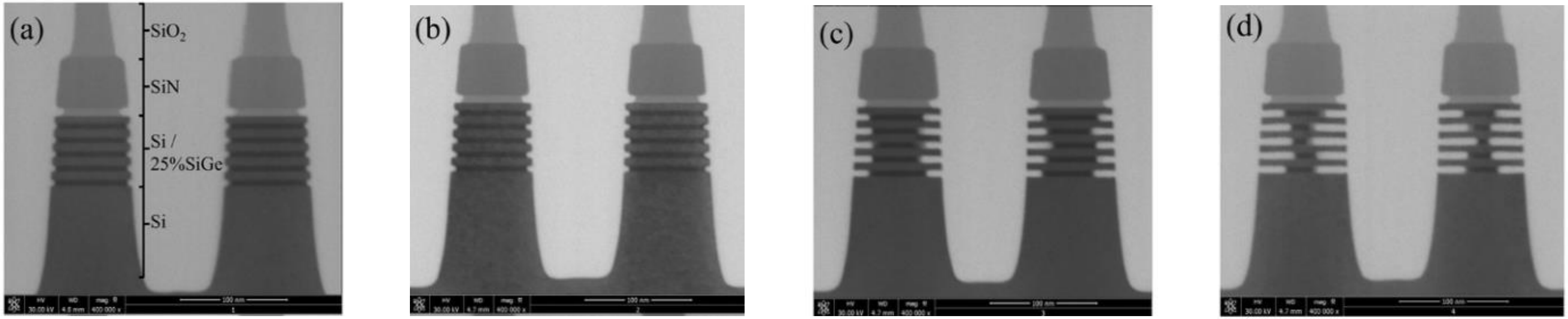
- Currently done with various dry etch processes some of them cyclic (passivation / etch)
- Selective native oxide removal before recess (vapor etch or ALE)
- SiGe ALE process: Abdulagatov et al. JVST A 39, 022602 (2021)



Zhao EDTM 2021

Si SiGe Metal 1 Metal 2 SOC High k W SiO_2 SiN SiCO(N)

Thermal Etching of SiGe with F_2 Gas



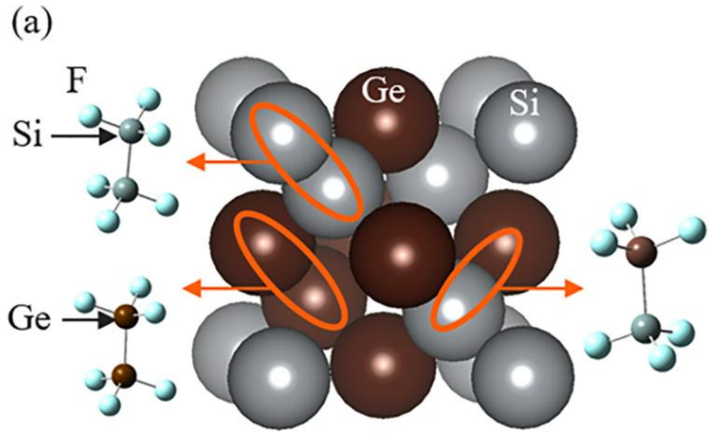
t=20s t=40s t=60s t=80s

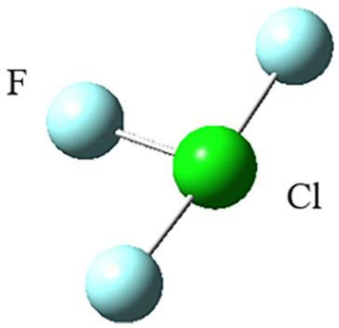
Partial pressure of F_2 is 6 mTorr. The temperature is 40℃.

Zajo et al., J. Vac. Sci. Technol. A **43**, 013007 (2025).

Knudsen transport, small sticking coefficient, only small fraction of incoming F_2 reacts with SiGe: Good top to bottom performance.

Thermal Etching of SiGe with ClF_3 Gas





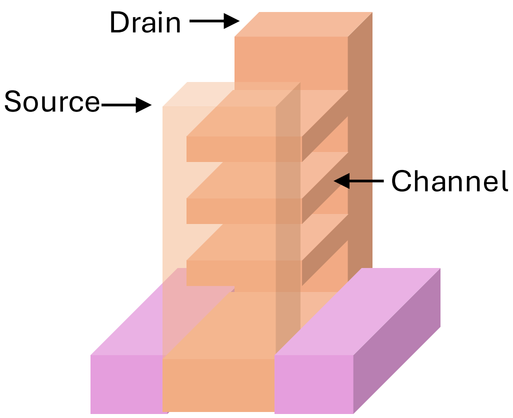
Findings from DFT computations:

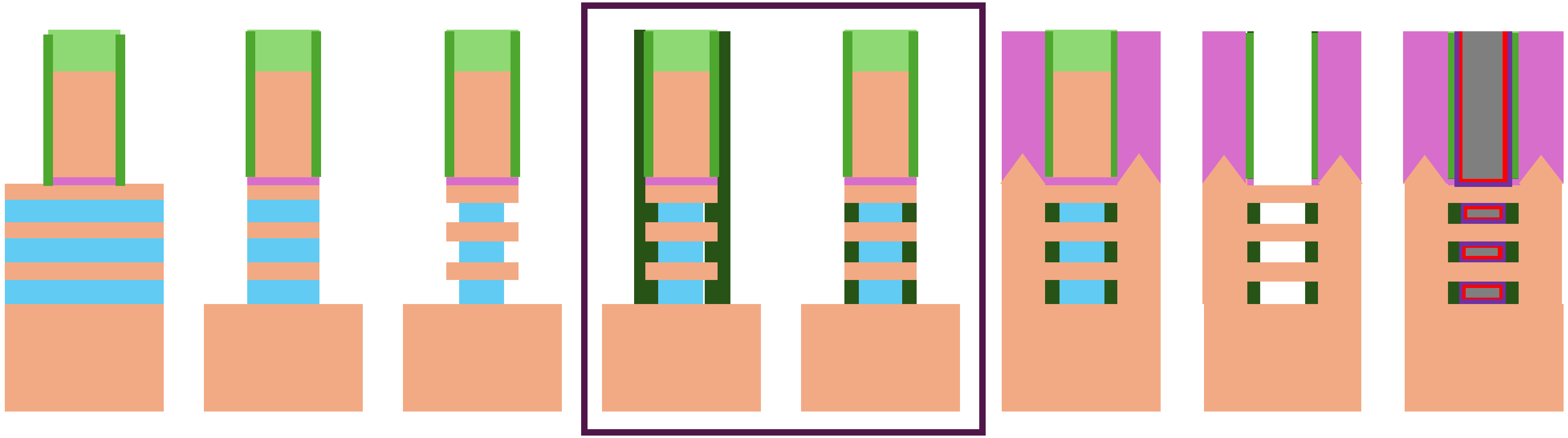
- Incorporation of Ge atom into the Si lowers fluorination E_a
- Double-F-transfer is predicted on the Ge-only and SiGe structures with the Ge atom being the front atom. The reaction results in a more negative ΔE and lower Ea than does the single-F-transfer
- Ge atom located on the second- and third-nearest-neighbor sites can still lower the E_a of the fluorination reaction. This indicates feasibility SiGe:Si selective etching with low Ge concentration.
- ClF_3 dissociating and creating F radicals, it is more likely to happen when fluorinating Si than a Ge atom. Reducing F radicals possibly formed near the surface may help protect an Si front.

Y. Tsai, M. Wang, J. Vac. Sci. Technol. B **40**, 013201 (2022).

Logic Devices: Nanosheet Inside Spacer Etch (SiN)

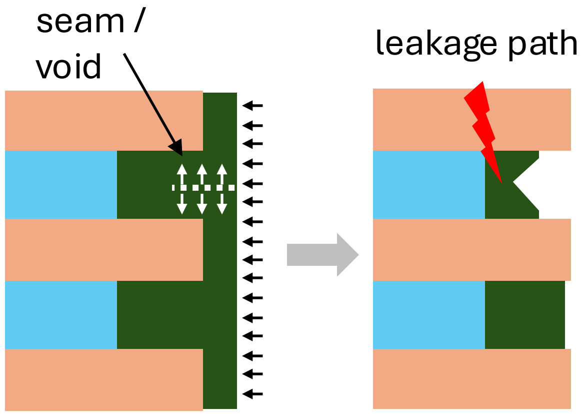
Target structure:





Requirements:

- Selectivity to Si, hardmask, hardmask spacer
- Top to bottom uniformity
- Insensitivity to seams

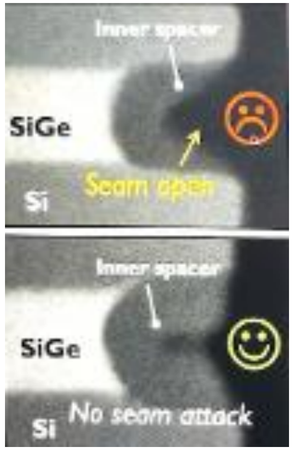


Post ALD: SiN, SiO_2, SiCO, bi-layer

Post Etch

Solutions:

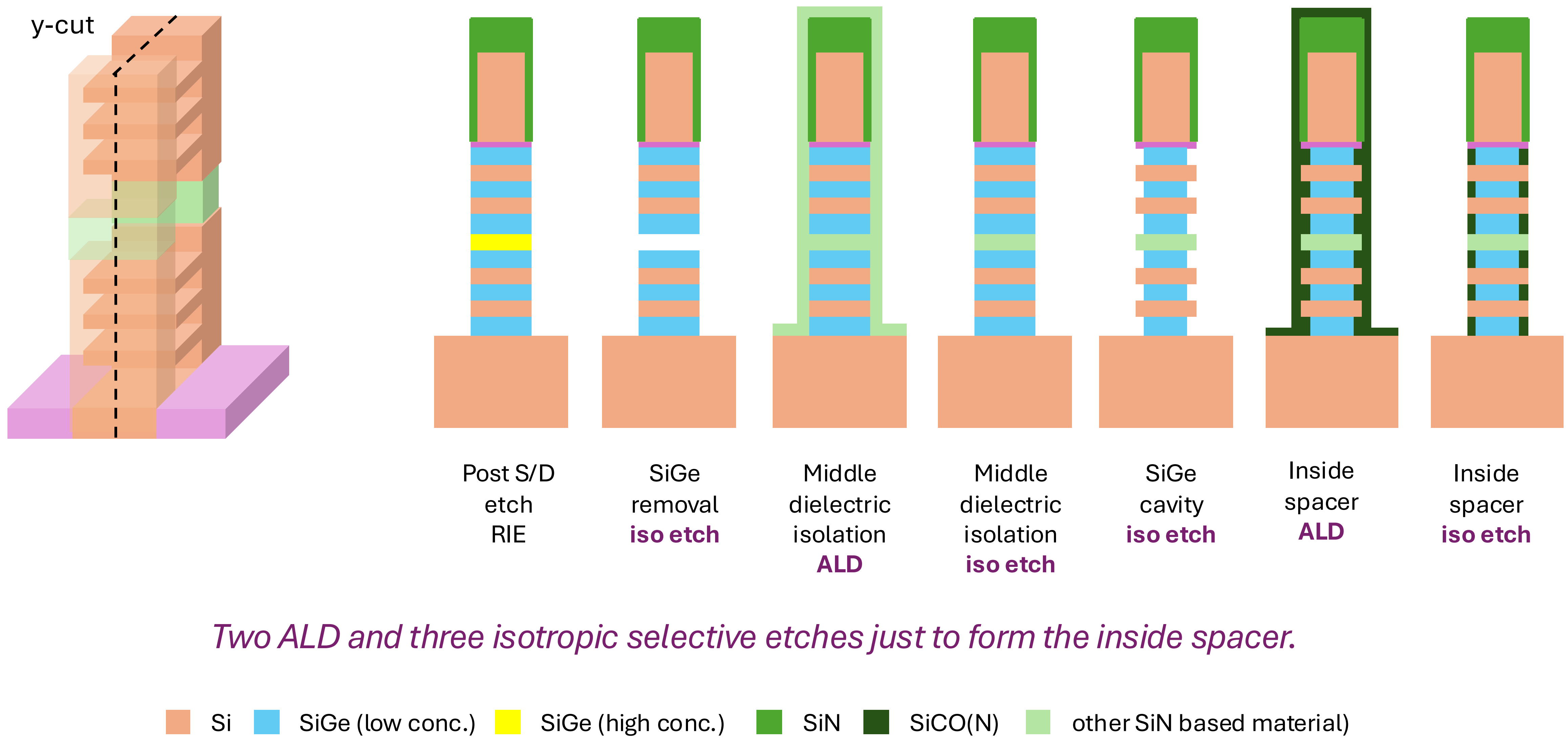
- ALD without seams
- ALE with undersaturated steps
- ALE with modification step with expanding volume



Y. Oniki SPCC 2020

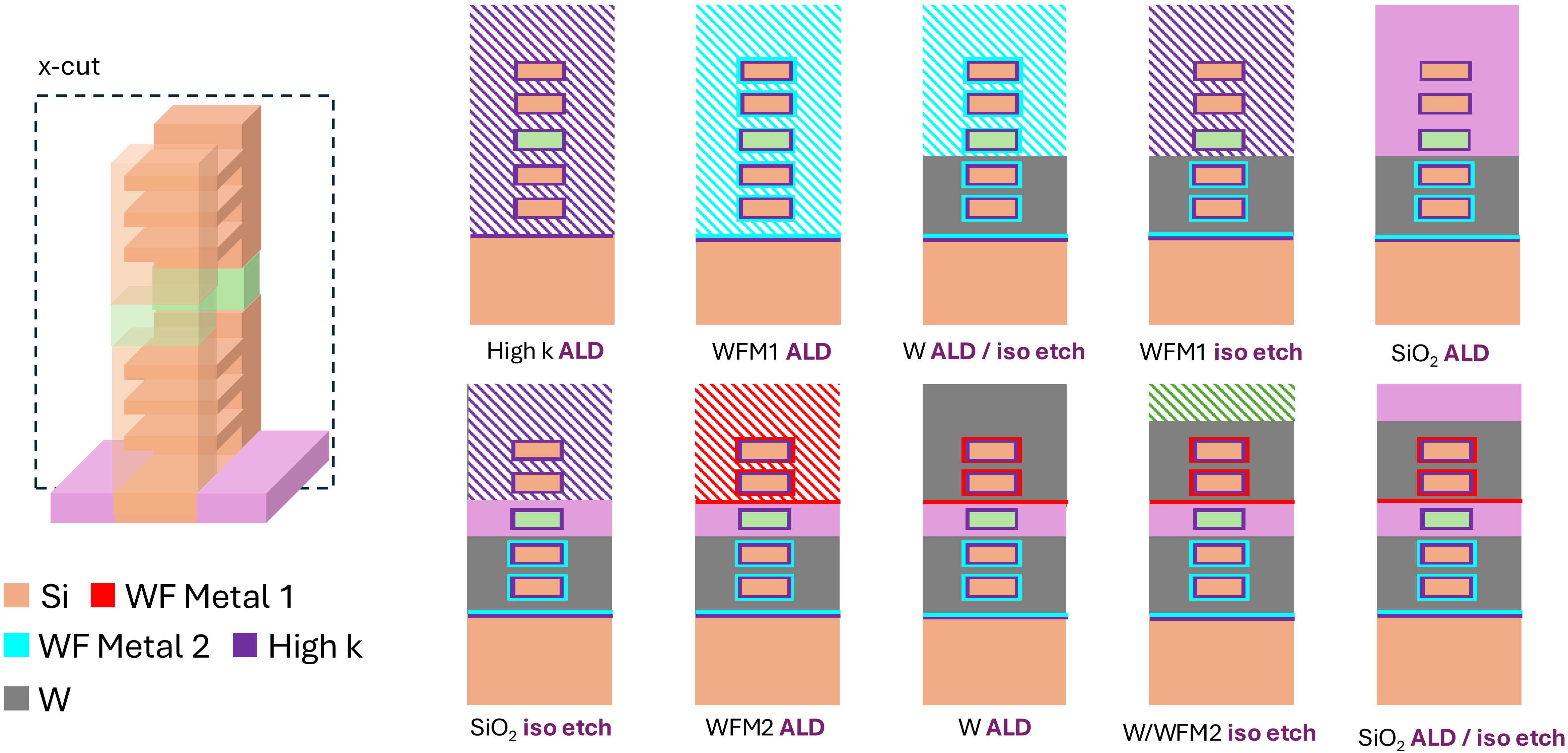
Si | SiGe | Metal 1 | Metal 2 | SOC | High k | W | SiO_2 | SiN | SiCO(N)

Logic Devices: CFET Inside Spacer with MDI



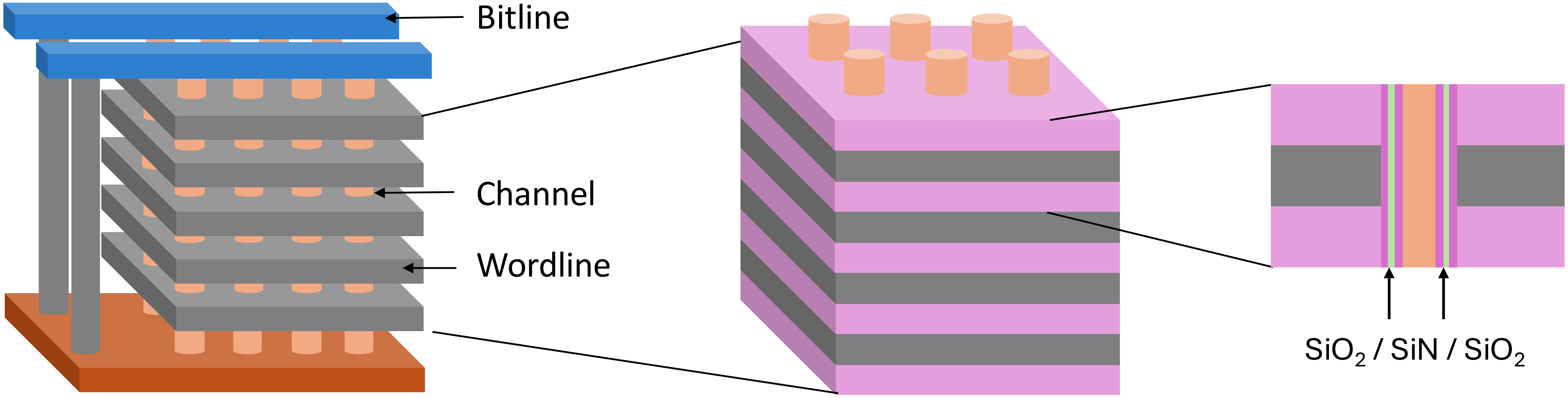
Two ALD and three isotropic selective etches just to form the inside spacer.

Logic Devices: Workfunction metals



6 ALD and 5 isotropic selective etches to forn high k / metal gates.

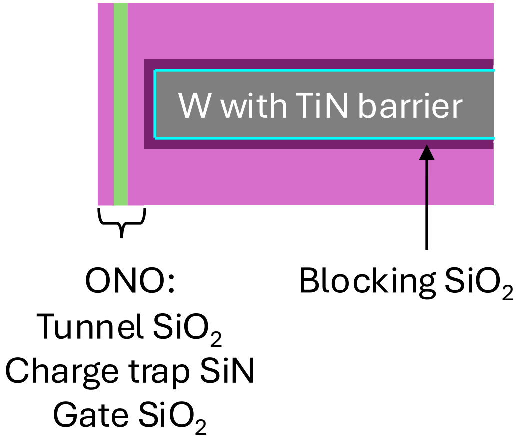
3D NAND ALD Opportunity: ONO



Charge trap ONO layer drive ALD deposition as aspect ratios increase.

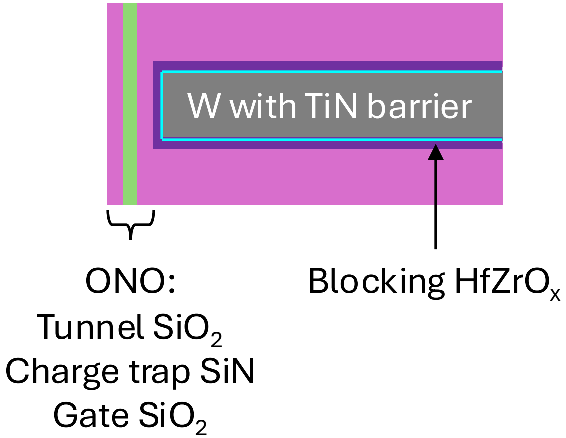
3D NAND ALD / ALE Opportunities: Ferroelectric Blocking and Charge Trap Layers

Conventional NAND



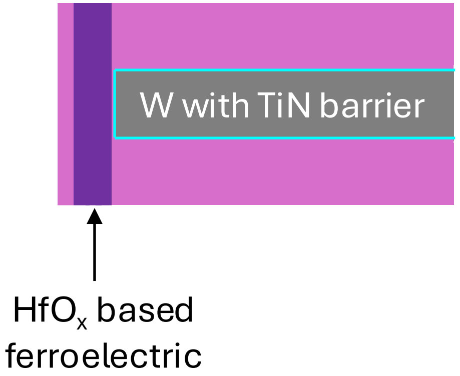
With Anti-Ferroelectric Blocking Layer

Shin et al., IEDM 2020

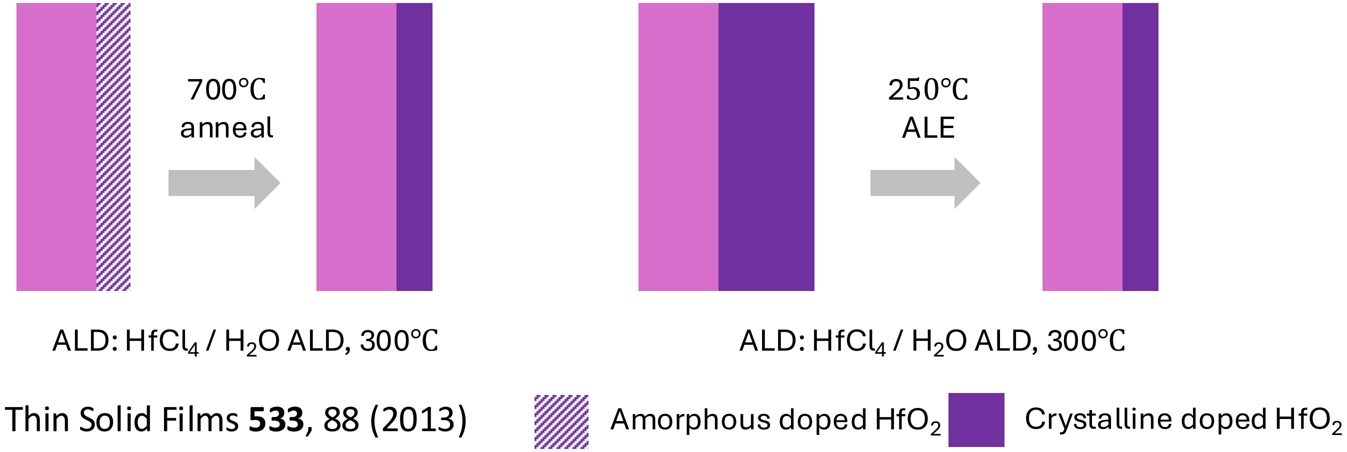


Ferroelectric NAND

Yoon et al., VLSI 2023



Formation of thin ferroelectric doped HfO_x:



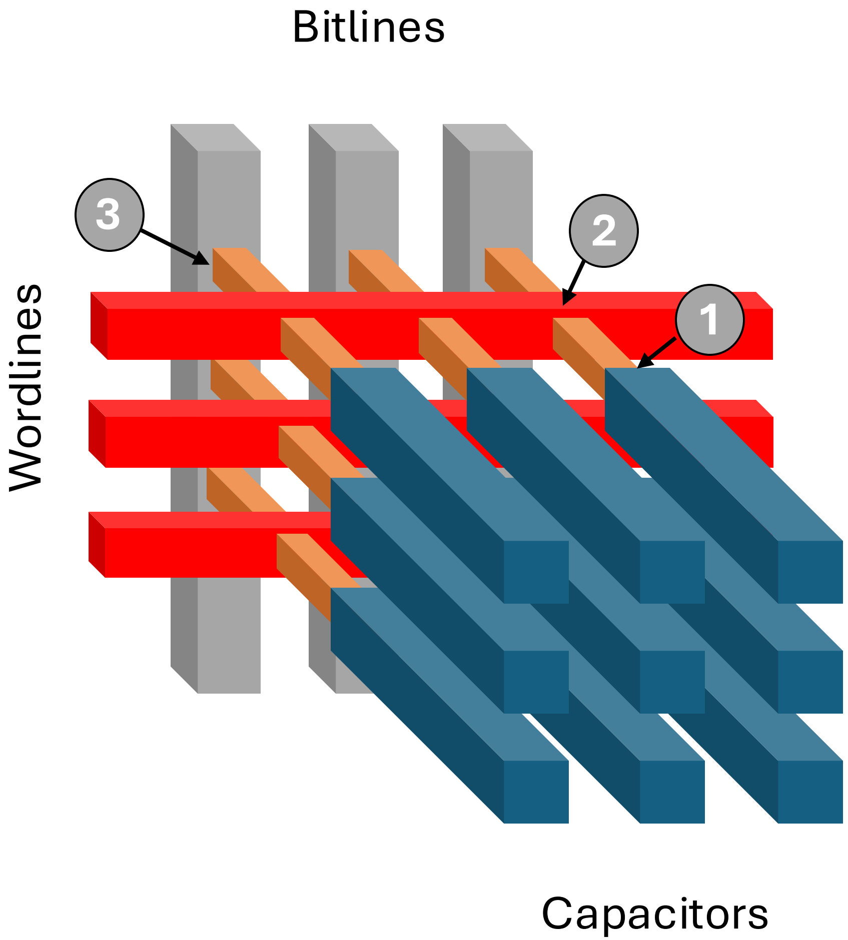
ALD: $HfCl_4$ / H_2O ALD, 300℃

ALD: $HfCl_4$ / H_2O ALD, 300℃

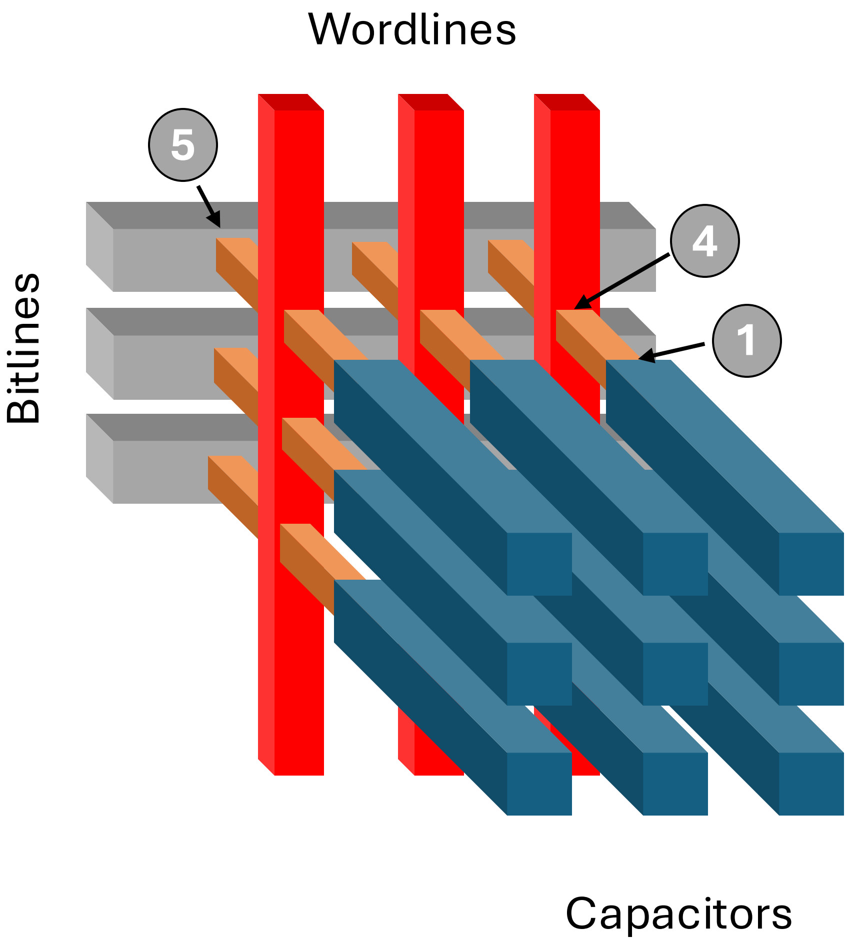
Yurchuk et al., Thin Solid Films **533**, 88 (2013)

Switch to ferroelectric HfO_x blocking and charge trap layers and ferroelectric device may drive need for ALD. This ferroelectric films can be realized combining ALD and ALE.

3D DRAM / VDRAM: Vertical and Horizontal Bitline Implementations



Vertical Bitline Scheme (VBL)

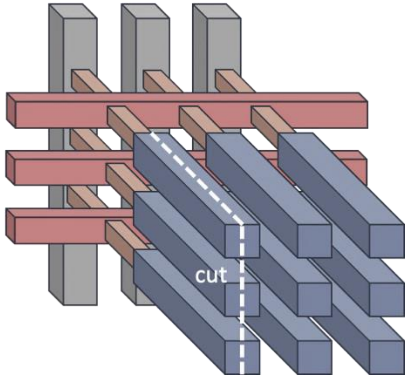


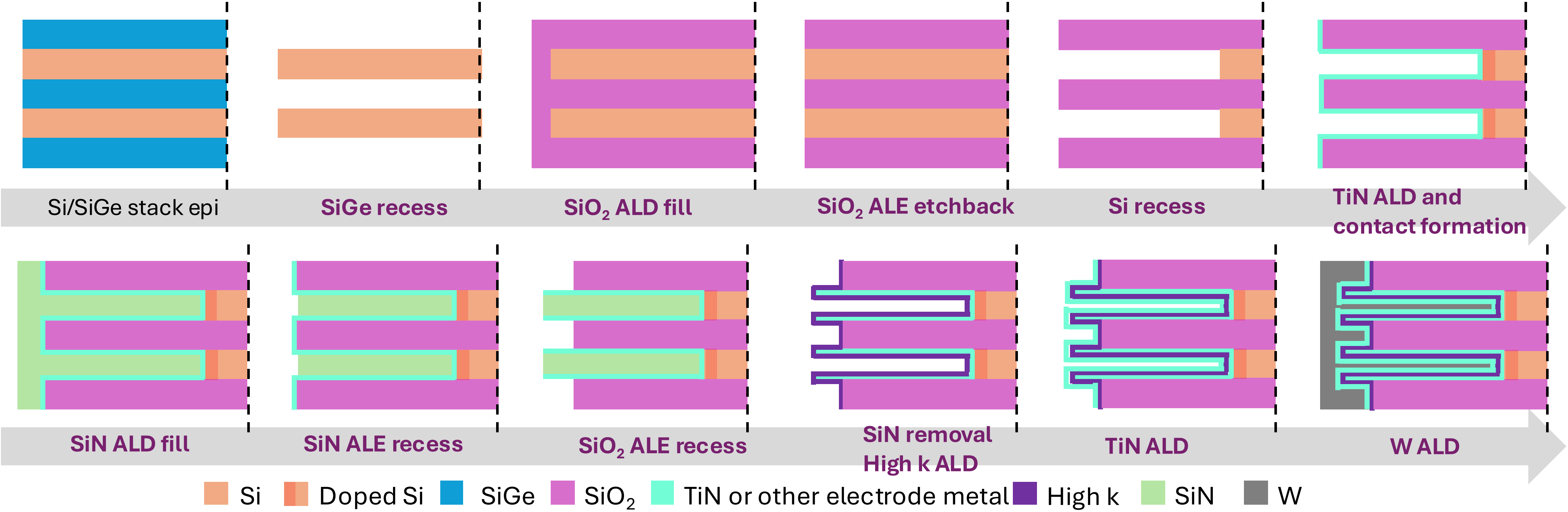
Horizontal Bitlines\ Scheme (HBL)

1	Capacitor
2	Horizontal Wordline
3	Vertical Bitline
4	Vertical Wordline
5	Horizontal Bitline

3D DRAM integration requires many lateral processing steps with ALD, ALE and thermal etching.
In contrast to logic devices, 3D DRAM features many very long lateral building blocks such as capacitors.

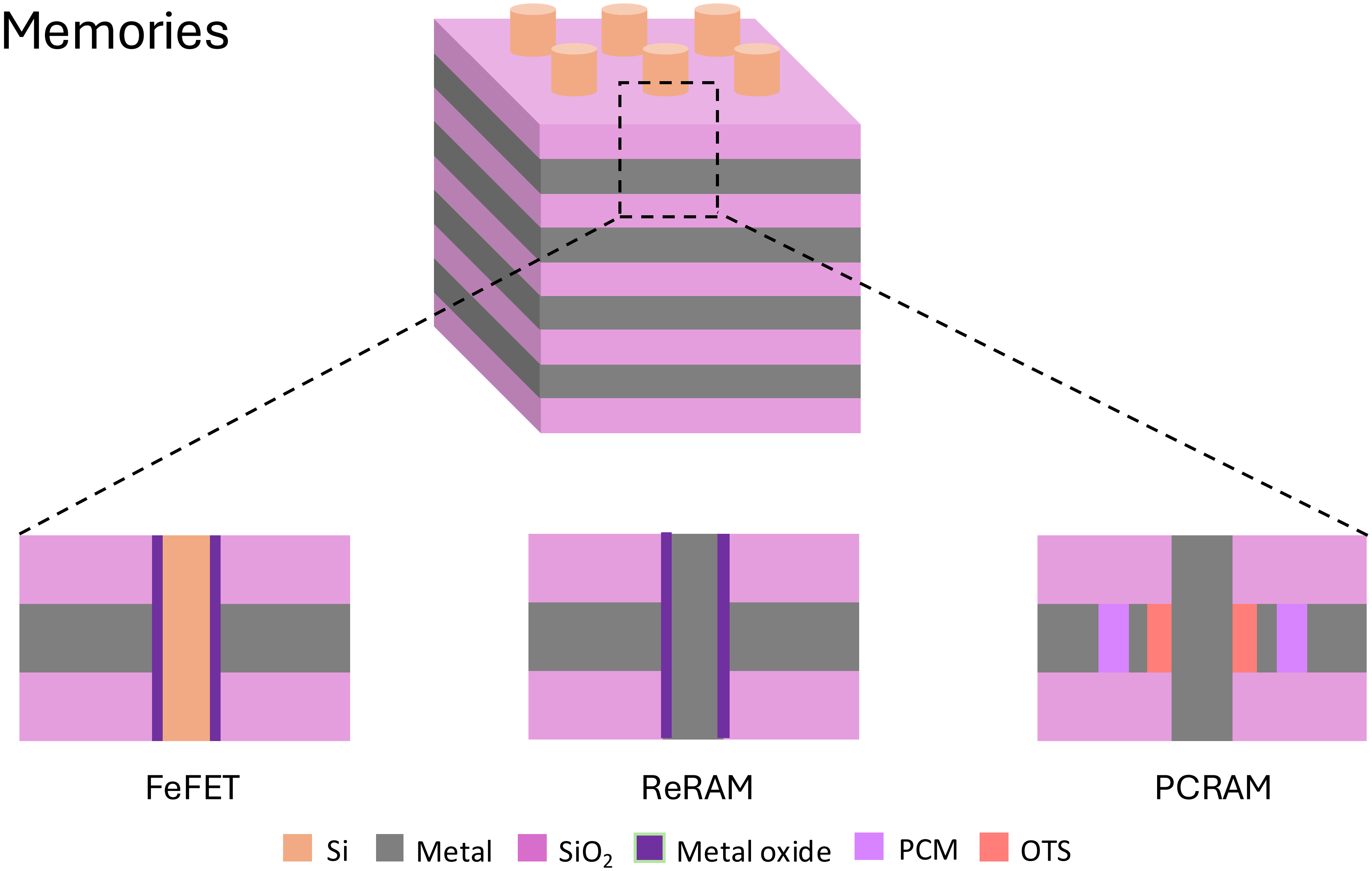
VDRAM Capacitor Integration





6 ALD and 6 isotropic selective etches to forn high k / metal gates.

Emerging Memories



Combination of ALD and ALE can be used to improve cell separation in PCRAM and RRAM memories.

Summary

- 3D integration requires high fidelity patterning, vertical and lateral etch and deposition.
- High fidelity patterning is enabled by ALD and directional ALE.
- The high aspect ratio scaffolds for 3D devices are made of conventional materials.
- The deposition and etch processes for realizing high aspect ratio scaffolds require very high deposition and etching rates. One of the innovations is cryo etching.
- Lateral integration is achieved by alternating ALD and selective isotropic etching processes.
- Among the isotropic etching processes, ALE allows etching of traditionally "hard to etch" materials and excellent top to bottom etch rate uniformity. The drawback is low etching rate.
- Device integration benefits from knowledge of the performance characteristics of all the deposition and etching technologies.